

# Datasheet

**APM32F030x4x6x8**

**Arm® Cortex®-M0+ based 32-bit MCU**

Version: V1.5

# 1. Product characteristics

## ■ System Architecture

- 32-bit Arm® Cortex®-M0+core
- Up to 48MHz working frequency

## ■ Memory

- Flash: 16~64Kbytes
- SRAM: 4~8Kbytes

## ■ Clock, reset and power management

- External supply voltage:  $V_{DD} = 2.0 \sim 3.6V$
- Analog power supply:  $V_{DDA} = V_{DD} \sim 3.6V$
- Power-on/power-down reset (POR/PDR)
- 4~32MHz crystal oscillator
- RTC 32KHz oscillator with calibration
- Internal 40 KHz RC oscillator

## ■ Low power consumption mode

- Sleep, halt and standby

## ■ Up to 55 fast I/O pins

- Supports all mappable external interrupt vectors
- Almost all I/O pins are compatible with 5V input

## ■ 5-channel DMA controller

## ■ Analog peripherals

- 1 12-bit ADC; up to 16 external channels supported, conversion range: 0 ~ 3.6V, independent analog power supply: 2.4~3.6V

## ■ Real-time clock RTC

- Support calendar function
- It can be used for alarm and periodic wake-up in halt and standby mode

## ■ 10 timers

- 1 16-bit advanced control timer with 7-channel PWM output
- Up to 5 general-purpose 16-bit timers
- 1 16-bit basic timer
- Independent watchdog and system window watchdog timer
- System tick timer

## ■ Communication interfaces

- Up to 2 I2C interfaces
- Up to 2 USART interfaces
- Up to 2 SPI interfaces

## ■ CRC calculation unit

## ■ Serial wire debugging (SWD)

## ■ 96-bit UID

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## 2. Brief introduction

The APM32F030x4x6x8 series chips are 32-bit high-performance microcontrollers based on Arm® Cortex®-M0+core, and the working frequency can reach 48MHz. Built-in high-speed memory (up to 64 kbytes of flash memory and 8 kbytes of SRAM), the chip pins are multiplexed with a large number of enhanced peripherals and I/O. All chips provide standard communication interfaces: I2C interface, SPI interface and USART interface.

The working temperature range of APM32F030x4x6x8 microcontroller is -40°C ~+105°C, and the voltage range is 2.0~3.6V. Many power-saving modes ensure the requirements of low-power applications.

The APM32F030x4x6x8 microcontroller includes many different packages with 20, 28, 32, 48 and 64 pins, and different package forms make the peripheral configuration of the device different.

For information about the Arm® Cortex®-M0+core, please refer to the Arm® Cortex®-M0+technical reference manual, which can be downloaded from ARM's website.

### 3. Function description

See the following table for specific APM32F030x4x6x8 product functions and peripheral configuration.

**Table 1 The functions and peripherals of APM32F030x4x6x8 series chips**

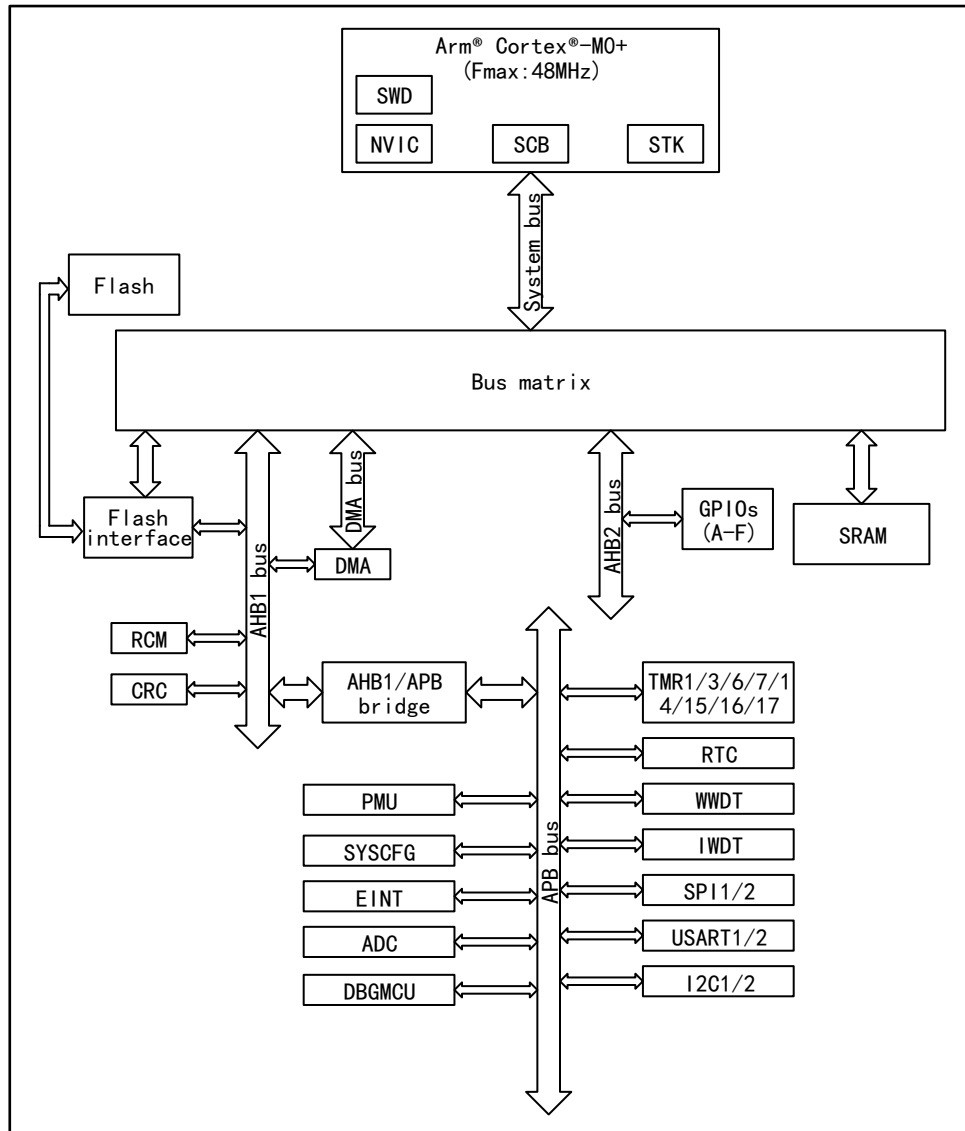
| Products                |                     | APM32F030 |      |      |       |      |      |       |        |      |       |      |        |      |        |    |
|-------------------------|---------------------|-----------|------|------|-------|------|------|-------|--------|------|-------|------|--------|------|--------|----|
| Model                   |                     | F4P6      | F6P6 | F8P6 | G4U6  | G6U6 | G8U6 | K6U6  | K6T6   | K8T6 | C6U6  | C8U6 | C6T6   | C8T6 | R8T6   |    |
| Encapsulation           |                     | TSSOP20   |      |      | QFN28 |      |      | QFN32 | LQFP32 |      | QFN48 |      | LQFP48 |      | LQFP64 |    |
| Flash memory (KB)       |                     | 16        | 32   | 64   | 16    | 32   | 64   | 32    |        | 64   | 32    | 64   | 32     | 64   |        |    |
| SRAM(KB)                |                     | 8         |      |      |       |      |      |       |        |      |       |      |        |      |        |    |
| Timer                   | 16-bit universal    | 4         |      |      |       |      | 5    |       |        |      |       |      |        |      |        |    |
|                         | 16-bit advanced     | 1         |      |      |       |      |      |       |        |      |       |      |        |      |        |    |
|                         | 16-bit Basic        | 0         |      |      | 1     |      |      |       |        |      |       |      |        |      |        |    |
|                         | 24-bit down counter | 1         |      |      |       |      |      |       |        |      |       |      |        |      |        |    |
|                         | Watchdog (WDT)      | 2         |      |      |       |      |      |       |        |      |       |      |        |      |        |    |
|                         | Real-time clock     | 1         |      |      |       |      |      |       |        |      |       |      |        |      |        |    |
| communication interface | USART               | 1         |      |      |       | 2    |      | 1     |        |      |       | 2    | 1      | 2    |        |    |
|                         | SPI                 | 1         |      |      |       |      | 2    | 1     |        |      |       | 2    | 1      | 2    |        |    |
|                         | I2C                 | 0         |      |      | 1     | 2    | 1    |       |        |      | 2     | 1    | 2      |      |        |    |
| 12-bit ADC              | Unit                | 1         |      |      |       |      |      |       |        |      |       |      |        |      |        |    |
|                         | External channel    | 9         |      |      | 10    |      |      |       |        |      |       |      |        |      |        | 16 |
|                         | Internal channel    | 2         |      |      |       |      |      |       |        |      |       |      |        |      |        |    |
| GPIOs                   |                     | 15        |      |      | 23    |      |      | 27    | 25     |      | 39    |      |        |      | 55     |    |

| Products              | APM32F030                                                                                        |
|-----------------------|--------------------------------------------------------------------------------------------------|
| Maximum CPU frequency | M0+@48MHz                                                                                        |
| Ambient temperature   | Ambient temperature: -40°C至 85°C/-40°C至 105°C<br>Junction temperature: -40°C至 105°C/-40°C至 125°C |
| Working voltage       | 2.0~3.6V                                                                                         |



### 3.1. System block diagram

Figure 1 System block diagram



### 3.2. Core

The Arm® Cortex®-M0+core is the latest generation of embedded Arm core. It is a low-cost platform, and APM32 is developed based on this platform, which has made a lot of optimization for system power consumption, while APM32 provides excellent computing performance and advanced system interrupt response.

The APM32F0xx series is based on the embedded ARM core, so it is compatible with all ARM tools and software.

The functional block diagram of APM32F030x4x6x8 series products is shown in figure 1.

### 3.3. Memory

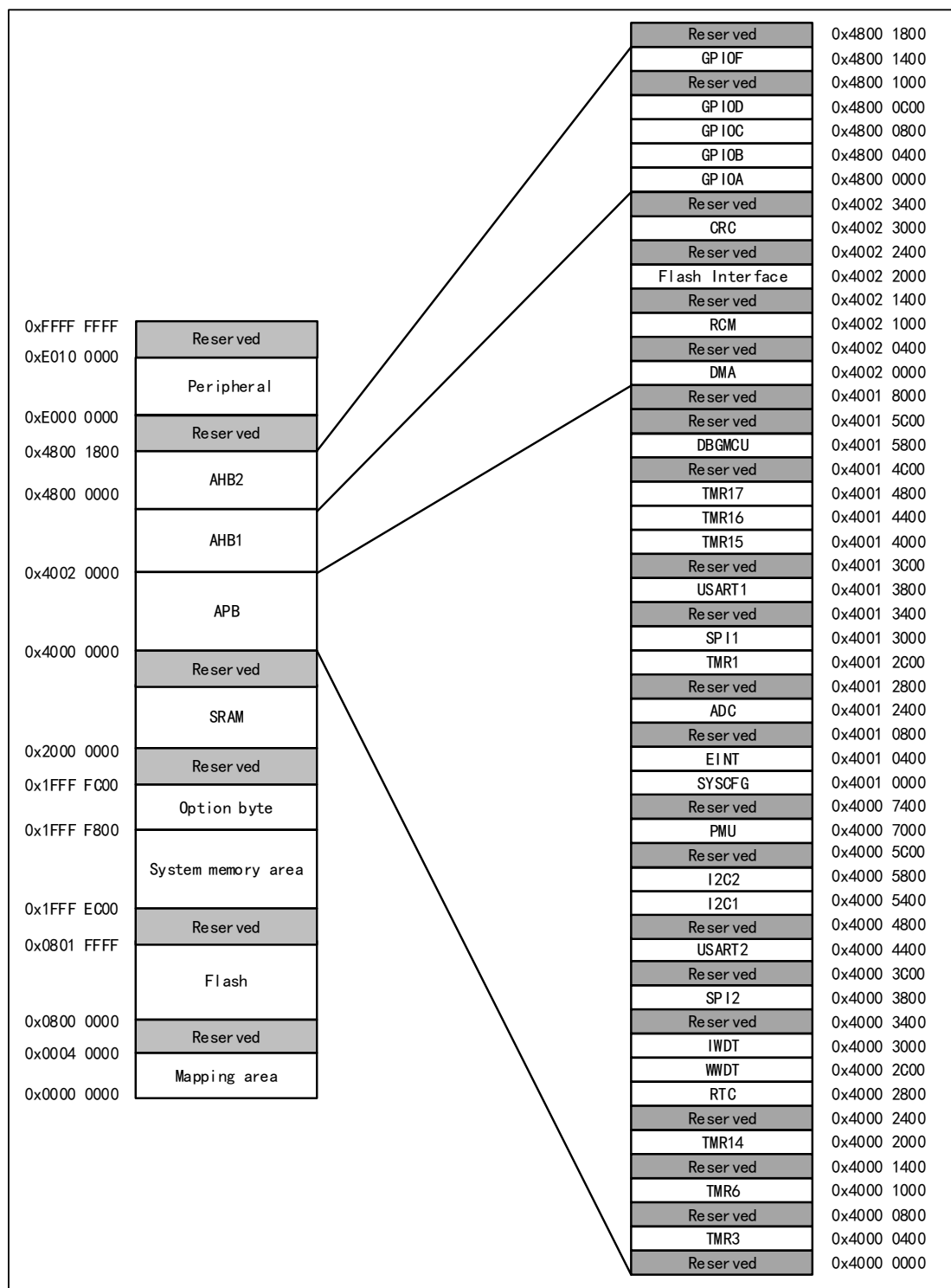
See the following table for memory details:

Table 2 Memory description

| Memory                | Max bytes | Function                                                     |
|-----------------------|-----------|--------------------------------------------------------------|
| Embedded flash memory | 64Kbytes  | Used to store programs and data                              |
| SRAM                  | 8Kbytes   | Used to store temporary data                                 |
| Option byte           | 16bytes   | Used to write protect memory and to protect the whole memory |

### 3.4. Address mapping

Figure 2 APM32F030x4x6x8 memory map



## 3.5. Power management

### 3.5.1 Power supply scheme

Table 3 Power supply scheme

| Name             | Voltage range         | description                                                                                                                                                                                                                |
|------------------|-----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| V <sub>DD</sub>  | 2.0~3.6V              | V <sub>DD</sub> directly supplies power to IO port, and V <sub>DD</sub> supplies power to core circuit through voltage regulator                                                                                           |
| V <sub>DDA</sub> | V <sub>DD</sub> ~3.6V | V <sub>DDA</sub> supplies power to ADC, reset module, RC oscillator and PLL. The V <sub>DDA</sub> voltage level must always be greater than or equal to the V <sub>DD</sub> voltage level, and it should be given priority |

Note: See Figure 9 (Power Supply Scheme) for more details on how to connect power supply pins.

### 3.5.2 Voltage regulator

There are three main modes of voltage regulator. The working mode of MCU can be adjusted by voltage regulator to reduce power consumption. See the following table for details of the three modes.

Table 4 Operation mode of voltage regulator

| Name                 | description                                                                                                                                                                                                                                  |
|----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Master mode (MR)     | Used in normal operation mode.                                                                                                                                                                                                               |
| Low power mode (LPR) | It can be used in halt mode when power demand decreases.                                                                                                                                                                                     |
| Power-down mode      | Used in power standby mode, the output of the voltage regulator is high impedance, the power supply of the core circuit is cut off, the voltage regulator is in zero consumption state, and all the data of registers and SRAM will be lost. |

Note: The voltage regulator is always in working state after reset, and outputs with high impedance in power-down mode.

### 3.5.3 Power supply monitor

Two circuits of power-on reset (POR) and power-down reset (PDR), are integrated inside the product. These two circuits are always in working condition. When the power-down reset circuit monitors that the power supply voltage is lower than the specified threshold V<sub>POR/PDR</sub>, the system enters the reset state, so it does not need to use an external reset circuit.

For details of V<sub>POR/PDR</sub>, please refer to 5. Test Conditions, Low Power Consumption Mode.

The APM32F0xx series supports the following three low power consumption modes, which can be configured by users to meet the best application requirements.

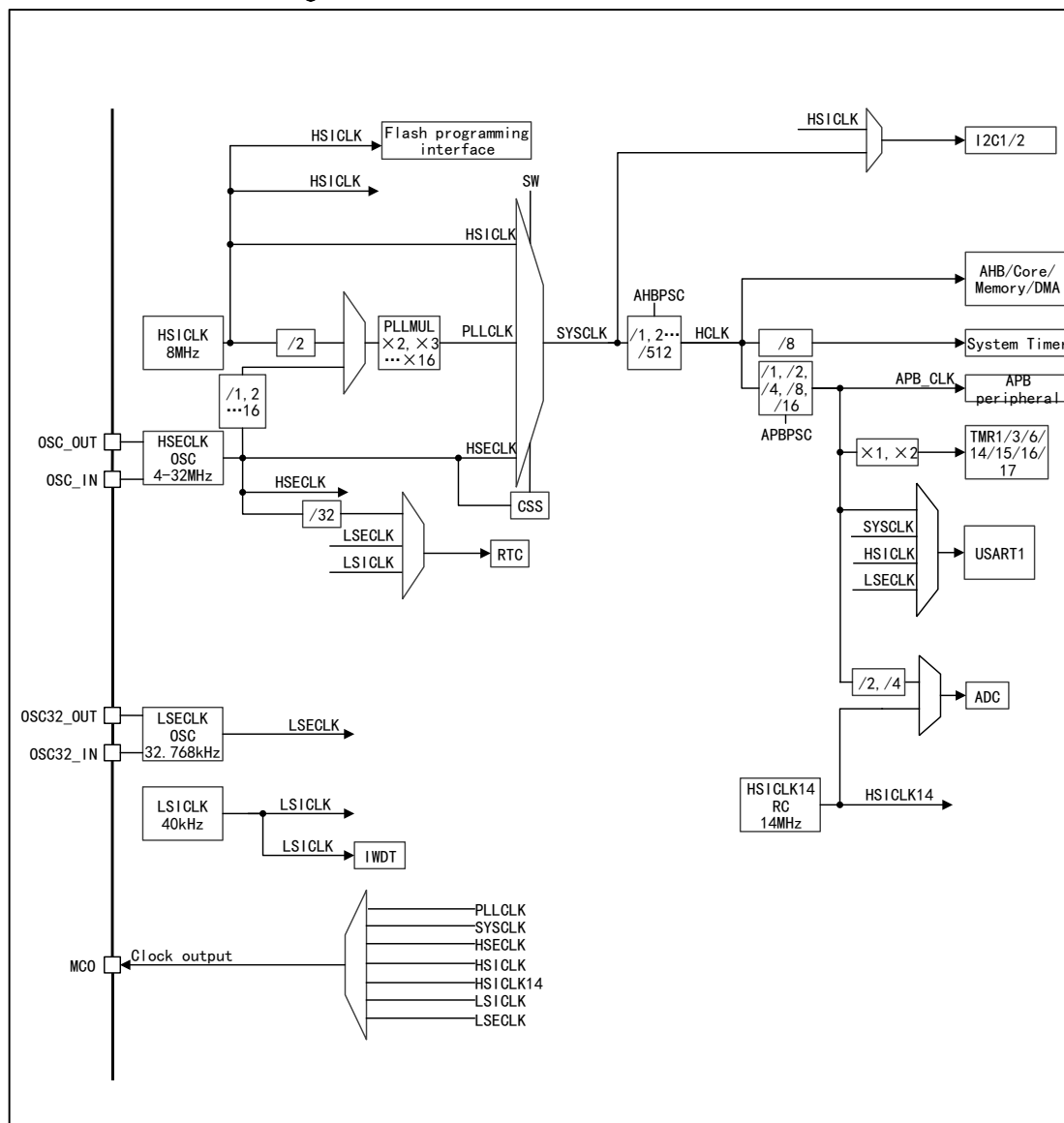
**Table 5 Low power consumption mode**

| Mode type    | description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Sleep mode   | In sleep mode, the CPU stops working, all peripherals are in working state, and interrupts/events can wake up the CPU.                                                                                                                                                                                                                                                                                                                                                                                                                                |
| halt mode    | <p>halt mode can achieve the lowest power consumption mode without losing SRAM and register data.</p> <p>At this time, the internal 1.5V power supply is stopped, which causes the clocks of HSECLK, HSICLK and PLL to turn off, and the voltage regulator is placed in normal mode or low power consumption mode.</p> <p>Interrupt and event wake-up configured as EINT can wake up CPU from halt mode. EINT signal includes one of 16 external I/O ports, RTC alarm clock or USB wake-up signal.</p>                                                |
| Standby mode | <p>Standby mode is the lowest power consumption mode used by the chip. At this time, the internal voltage regulator is turned off, which causes the power supply of the internal 1.5V part to be cut off, and the clocks of HSECLK, HSICLK and PLL are turned off; SRAM and register data will also disappear. However, the contents of the backup register remain, and the standby circuit still works.</p> <p>The external reset signal on NRST, IWDG reset, a rising edge on WKUP pin or RTC alarm clock will terminate the chip standby mode.</p> |

**Note: RTC, IWDG and corresponding clocks still work normally in halt or standby mode.**

### 3.6. Clock tree

Figure 3 Clock tree of APM32F030x4x6x8



### 3.7. Clock and startup

Users can use 4~32MHz external high-speed clock with "failure monitoring" function through configuration. When the system clock does not detect that the external clock is configured, the system will automatically switch to the internal RC oscillator.

### 3.8. Real time clock (RTC)

RTC is an independent BCD timer/counter, which can not only support calendar function, but also have alarm clock interrupt and periodic interrupt function. Besides sub-second, second, minute, hour (12 or 24-hour format), week, date, month and year, the calendar clock existing in BCD (binary coded decimal system) format, the calendar function can also automatically adjust one month to 28, 29(leap year), 30 and 31 days.

Users can dynamically adjust RTC clock pulses from 1 to 32767. By adjusting RTC clock pulse to synchronize RTC and master clock, it can compensate the inaccuracy of quartz crystal, and the resolution of its digital calibration circuit is 1ppm. RTC has two programmable filter anti-tampering detection pins, which can wake up MCU in halt and standby modes when tampering events are detected. In addition, RTC has time stamp function, which can be used to save calendar contents. The timestamp function of RTC can be triggered by events on pins or tampering events. The MCU can wake up from the halt and standby modes when detecting a time event. The reference clock detection can use a more accurate second source clock (50 or 60Hz) to improve the accuracy of the calendar. Its clock source can be an external crystal oscillator, resonator or oscillator with 32.768kHz, an internal RC oscillator with low power consumption (typical frequency is 40KHz) or a high-speed external clock with 32 frequency division.

### 3.9. Startup mode

At startup, the user can select one of the following three startup modes by setting the high and low levels of the Boot pin:

- Startup from user Flash
- Startup from system memory
- Startup from embedded SRAM

Users can use USART to reprogram user Flash (ISP) when startup from system memory.

### 3.10. **CRC calculation unit**

A CRC (Cyclic Redundancy Check) calculation unit obtains a CRC code through a generator polynomial algorithm.

### 3.11. **Interrupt controller**

#### 3.11.1 **Nested Vector Interrupt Controller (NVIC)**

The APM32F030x4x6x8 product has a nested vector interrupt controller, and NVIC can handle up to 32 maskable interrupt channels (excluding 16 interrupt lines of Cortex®-M0+) and 4 priorities.

Nested Vector Interrupt Controller (NVIC) has a tightly coupled NVIC interface, which directly transmits the interrupt vector entry address to the kernel, thus achieving low-latency interrupt response processing. In addition, it can give priority to late arriving higher priority interrupts

#### 3.11.2 **External Interrupt/Event Controller (EINT)**

The external interrupt/event controller consists of 32 edge detectors that generate event/interrupt requests. Its trigger events (rising edge or falling edge or double edge) can be independently configured or shielded; There is a register that holds the status of all interrupt requests. Up to 55 general-purpose I/Os can be connected to 16 external interrupt lines. EINT can detect pulses whose width is smaller than the internal clock period.

### 3.12. **DMA**

Five flexible general-purpose DMA can transfer data from memory to memory, from peripheral to memory and from memory to peripheral. The DMA controller supports the management of the ring buffer, and when the controller reaches the end of the buffer, there is no need for user code intervention.

Each channel has special hardware DMA request logic, and each channel can be triggered by software, and the address and target address can also be set independently by software.



DMA can be used for major peripherals: SPI, I2C, USART, all TMRx timers (except TMR14) and ADC.

### 3.13. Timer

The APM32F030x4x6x8 product includes up to five general timers, a basic timer and an advanced control timer.

**Table 6 Advanced control timer**

| Timer type                     | Advanced control timer                                                                                                                                                                                                                                                                                                                                                                                               |
|--------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Timer                          | TMR1                                                                                                                                                                                                                                                                                                                                                                                                                 |
| Counter resolution             | 16 bits                                                                                                                                                                                                                                                                                                                                                                                                              |
| Counter type                   | Up, down, up/down                                                                                                                                                                                                                                                                                                                                                                                                    |
| Prescaler coefficient          | Any integer between 1 and 65536                                                                                                                                                                                                                                                                                                                                                                                      |
| DMA request generation         | Yes                                                                                                                                                                                                                                                                                                                                                                                                                  |
| Acquisition/comparison channel | 4                                                                                                                                                                                                                                                                                                                                                                                                                    |
| Complementary output           | Yes                                                                                                                                                                                                                                                                                                                                                                                                                  |
| Function description           | <p>It has complementary PWM output with dead band insertion, and can also be regarded as a complete general timer.</p> <p>When configured as a 16-bit standard timer, it has the same function as the TMRx timer.</p> <p>When configured as a 16-bit PWM generator, it has full modulation capability (0~100%).</p> <p>In debug mode, the timer can be frozen.</p> <p>Provides synchronization or event linking.</p> |

**Table 7 Basic timer**

| Timer type                     | Basic timer                                          |
|--------------------------------|------------------------------------------------------|
| Timer                          | TMR6                                                 |
| Counter resolution             | 16 bits                                              |
| Counter type                   | Up                                                   |
| Prescaler coefficient          | Any integer between 1 and 65536                      |
| DMA request generation         | Yes                                                  |
| Acquisition/comparison channel | 0                                                    |
| Complementary output           | -                                                    |
| Function description           | It can be used as a universal 16-bit time base clock |

**Table 8 General timer**

| Timer type                      | General timer                                                                                                                                                                                                                                                              |                                                                                               |                                                                                                                                                                                                                                                                                                                                                                                        |                                 |       |
|---------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------|-------|
| Timer                           | TMR3                                                                                                                                                                                                                                                                       | TMR14                                                                                         | TMR15                                                                                                                                                                                                                                                                                                                                                                                  | TMR16                           | TMR17 |
| Counter resolution              | 16 bits                                                                                                                                                                                                                                                                    | 16 bits                                                                                       | 16 bits                                                                                                                                                                                                                                                                                                                                                                                | 16 bits                         |       |
| Counter type                    | Up, down,<br>Up, down                                                                                                                                                                                                                                                      | Up                                                                                            | Up                                                                                                                                                                                                                                                                                                                                                                                     | Up                              |       |
| Prescaler                       | Any integer between 1 and 65536                                                                                                                                                                                                                                            | Any integer between 1 and 65536                                                               | Any integer between 1 and 65536                                                                                                                                                                                                                                                                                                                                                        | Any integer between 1 and 65536 |       |
| DMA request generation          | Yes                                                                                                                                                                                                                                                                        | No                                                                                            | Yes                                                                                                                                                                                                                                                                                                                                                                                    | Yes                             |       |
| Capture/<br>Comparison Channels | 4                                                                                                                                                                                                                                                                          | 1                                                                                             | 2                                                                                                                                                                                                                                                                                                                                                                                      | 1                               |       |
| Function description            | There are 4 independent channels, each for input capture/output comparison, PWM or single pulse mode output. Up to 12 input capture, output comparison or PWM channels can be provided in the largest package configuration. It has an independent DMA request generation. | Single channel, PWM or single pulse mode output function for input capture/output comparison. | It has complementary output function with dead zone generation and independent DMA request generation. These three timers can work together, and TMR15 operates with TMR1 through link function, which can realize synchronization or event link function. TMR15 has two independent channels, while TMR16 and TMR17 are synchronized. TMR15 can be synchronized with TMR16 and TMR17. |                                 |       |

**Table 9 Comparison between independent watchdog and window watchdog**

| Name                        | Counter Resolution | Counter type | Prescaler coefficient               | Function description                                                                                                                                                                                                                                                                                                                                        |
|-----------------------------|--------------------|--------------|-------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Independent watchdog (IWDG) | 12 bits            | down         | Between 1 and 256 Arbitrary integer | <p>The clock is provided by an internally independent RC oscillator of 40KHz, which is independent of the master clock, so it can run in halt and standby modes.</p> <p>The whole system can be reset in case of problems.</p> <p>You can provide timeout management for applications. It can be configured as a software or hardware startup watchdog.</p> |

| Name                   | Counter Resolution | Counter type | Prescaler coefficient | Function description                                                                                                                                                                              |
|------------------------|--------------------|--------------|-----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                        |                    |              |                       | In debug mode, the counter can be paused for convenience of debugging.                                                                                                                            |
| Window watchdog (WWDT) | 7 bits             | down         | -                     | It can be set to run freely.<br>The whole system can be reset in case of problems.<br>Driven by the master clock, it has early interrupt warning function.<br>Timers in debug mode can be frozen. |

### 3.14. System tick timer

System tick timer is a standard 24-bit down counter with automatic reloading function. When the counter is 0, it can generate a masked system interrupt and can program the clock source (HCLK or HCLK/8).

### 3.15. General purpose input/output interface (GPIO)

Each GPIO pin can be configured as an output (push-pull or open drain), an input (with or without pull-down) or a multiplexed peripheral function port by software. Most GPIO pins can be shared with digital or analog multiplexed peripherals.

The peripheral functions of I/O pins can be locked by a specific operation sequence to avoid accidental writing to I/O registers.

### 3.16. Communication interface

#### 3.16.1 I2C bus

I2C1/2 can work in master mode and slave mode, and supports 7-bit and 10-bit addressing modes. I2C1/2 supports standard mode (up to 100kbit/s) or fast mode (up to 400kbit/s). In addition, I2C1 has built-in programmable analog and digital noise filters, and also supports ultra-fast mode (up to 1 Mbit/s).

In addition, I2C1 also provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP function, host notification protocol, hardware CRC(PEC) generation/verification, timeout verification and alarm protocol management.

I2C supports DMA function.

See table 10 for the differences between I2C1 and I2C2.

**Table 10 APM32F030x4x6x8I2C function**

| I2C function                                                                 | I2C1             | I2C2 <sup>(2)</sup> |
|------------------------------------------------------------------------------|------------------|---------------------|
| 7-bit addressing mode                                                        | √ <sup>(1)</sup> | √                   |
| 10-bit addressing mode                                                       | √                | √                   |
| Standard mode (up to 100kbit/s)                                              | √                | √                   |
| Fast mode (up to 400kbit/s)                                                  | √                | √                   |
| Ultra-fast mode (up to 1Mbit/s), I/O port supports 20mA output current drive | √                | -                   |
| Independent clock                                                            | √                | -                   |
| SM bus                                                                       | √                | -                   |
| Wake up from halt                                                            | -                | -                   |

**Note:**

- (1) √ = support  
 (2) Available only on APM32F030x8 chip.

### 3.16.2 Universal synchronous/asynchronous transceiver (USART)

Up to two universal synchronous/asynchronous transceivers are built in the chip, and the communication rate can reach 6Mbit/s at the highest. All USART interfaces can be provided by DMA controller, and the functions that USART interfaces can realize are shown in the following table.

**Table 11 APM32F0x6/8 USART function**

| USART mode/function                          | APM32F030x6       | APM32F030x8 |        |
|----------------------------------------------|-------------------|-------------|--------|
|                                              | USART1            | USART1      | USART2 |
| Hardware flow control of modem               | √                 | √           | √      |
| Continuous communication using DMA           | √                 | √           | √      |
| Multiprocessor communication                 | √                 | √           | √      |
| Synchronization mode                         | √                 | √           | √      |
| Smart card mode                              | -                 | -           | -      |
| Single wire half duplex communication        | √                 | √           | √      |
| IrDA SIR codec module                        | -                 | -           | -      |
| LIN mode                                     | -                 | -           | -      |
| Dual clock domain and wake-up from halt mode | -                 | -           | -      |
| Receiver timeout interrupt                   | √                 | √           | -      |
| MODBUS communication                         | -                 | -           | -      |
| Auto baud rate detection (supported mode)    | 2                 | 2           | -      |
| USART data length                            | 8 bits and 9 bits |             |        |

**Note:** √ = support.

### 3.16.3 SPI

Two SPI interfaces are embedded in APM32F0xx series, which enables the chip to communicate with external devices in half/full duplex serial mode. The interface can be configured as master mode or slave mode. Eight master mode frequencies can be generated by a 3-bit prescaler, with 4~16 bits per frame and a communication rate of 18 Mbit/s.

The functions of SPI1 and SPI2 are similar, see the table below for details.

Table 12 **APM32F030x4x6x8 SPI function**

| SPI function                                    | SPI              | SPI2 <sup>(2)</sup> |
|-------------------------------------------------|------------------|---------------------|
| Calculation of hardware cyclic redundancy check | √ <sup>(1)</sup> | √                   |
| Receive/Send first in first out (FIFO)          | √                | √                   |
| NSS pulse mode                                  | √                | √                   |
| TI mode                                         | √                | √                   |

**Note:**

- (1) √ = supported.
- (2) Available only on APM32F030x8 chip.

## 3.17. Analog interface

### 3.17.1 ADC (analog/digital converter)

The 12-bit A/D converter has up to 16 external channels and 2 internal channels (temperature sensor, voltage reference), which can perform single or scanning conversion.

The analog watchdog function can monitor multiple channels very accurately, and when the monitored signal exceeds the threshold value, an interrupt will be generated.

ADC supports DMA function.

#### 3.17.1.1. Internal reference voltage ( $V_{REFINT}$ )

The internal reference voltage ( $V_{REFINT}$ ) provides a stable (band gap) voltage output for the ADC.  $V_{REFINT}$  is internally connected to the ADC\_IN17 input channel.

Table 13 **Internal reference voltage calibration value**

| Calibration value name | description                                                                   | Memory address            |
|------------------------|-------------------------------------------------------------------------------|---------------------------|
| VREFINT_CAL            | Original data collected at 30°C(± 5 °C)<br>and V <sub>DDA</sub> = 3.3v (10mv) | 0x1FFF F7BA - 0x1FFF F7BB |

### 3.17.1.2. Serial wire debug port (SW-DP)

The product provides ARM SW-DP interface, through which MCU can be connected with serial line debugging tool.

## 4. Pin characteristics

### 4.1. Pin definition

Figure 4 Pin definition diagram of APM32F030x4x6x8 series LQFP64

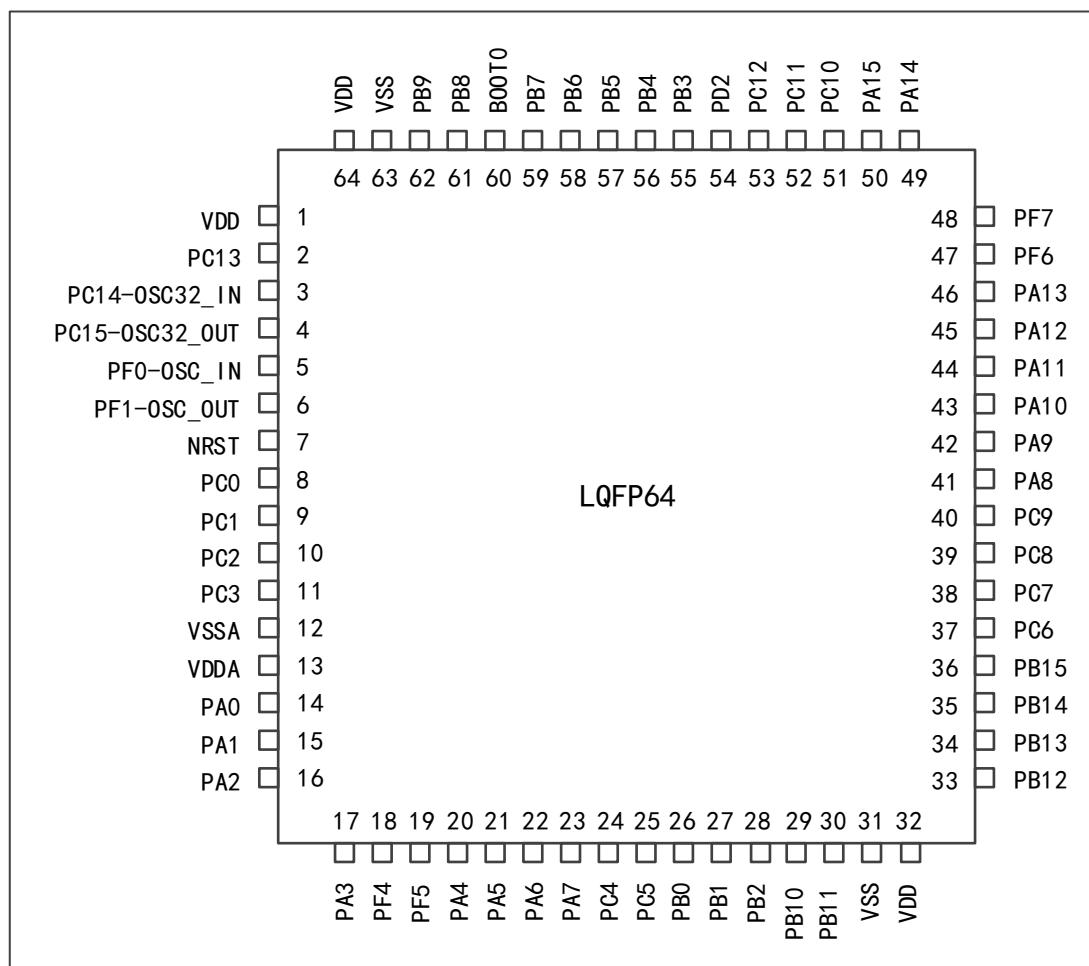


Figure 5 Pin configuration diagram of APM32F030x4x6x8 series LQFP48

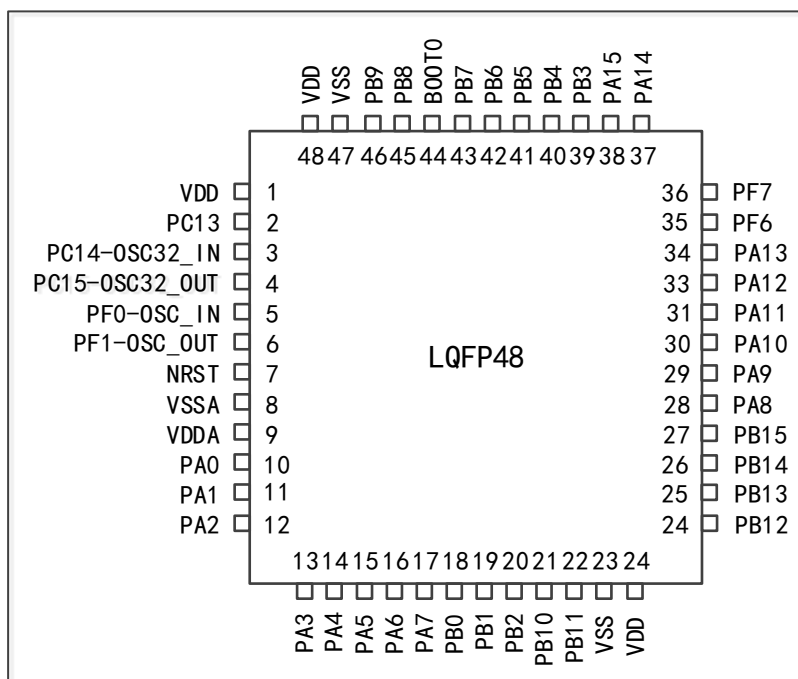


Figure 6 Pin configuration diagram of APM32F030x4x6x8 series LQFP32

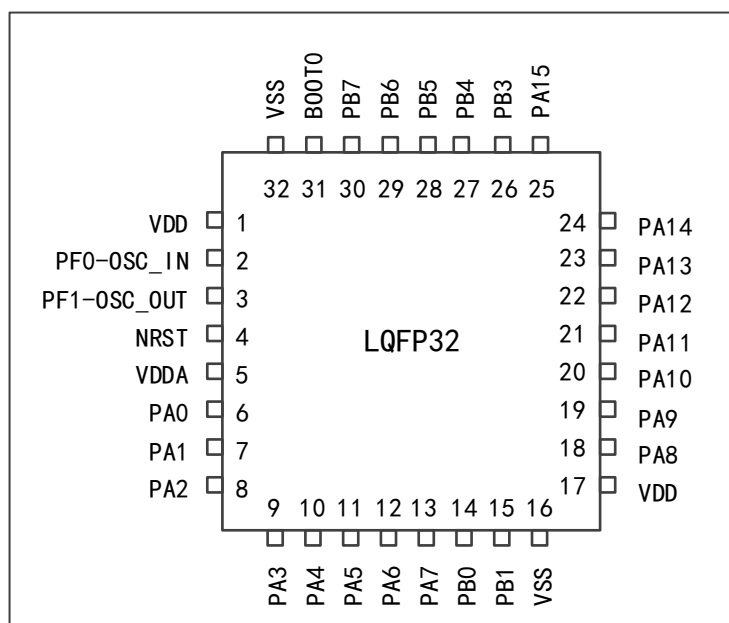




Figure 7 Pin configuration diagram of APM32F030x4x6x8 series QFN48

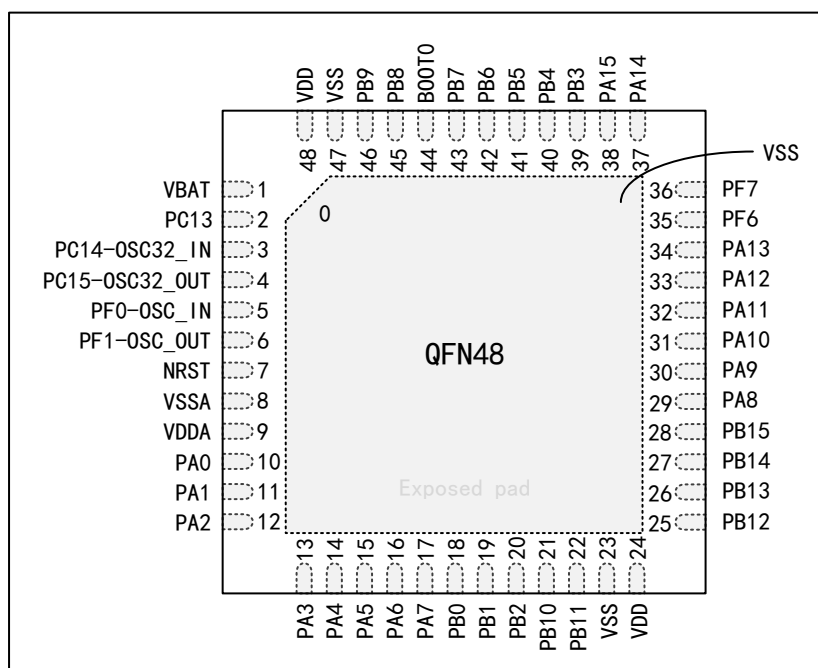


Figure 8 Pin configuration diagram of APM32F030x4x6x8 series QFN32

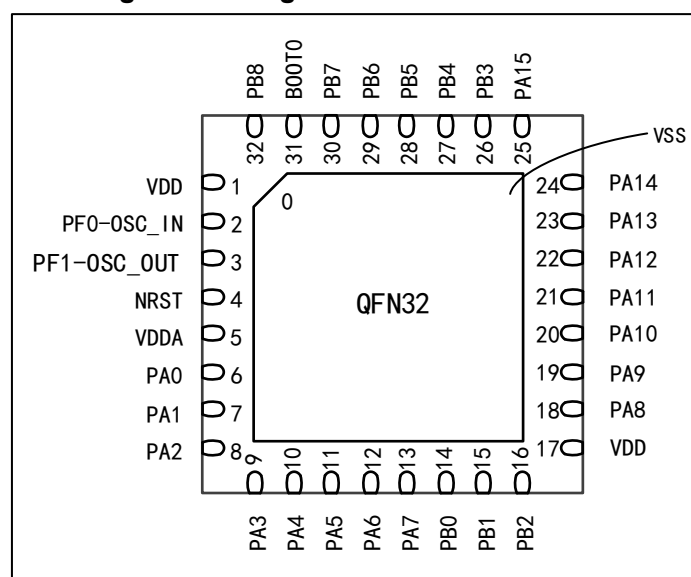


Figure 9 Pin configuration diagram of APM32F030x4x6x8 series QFN28

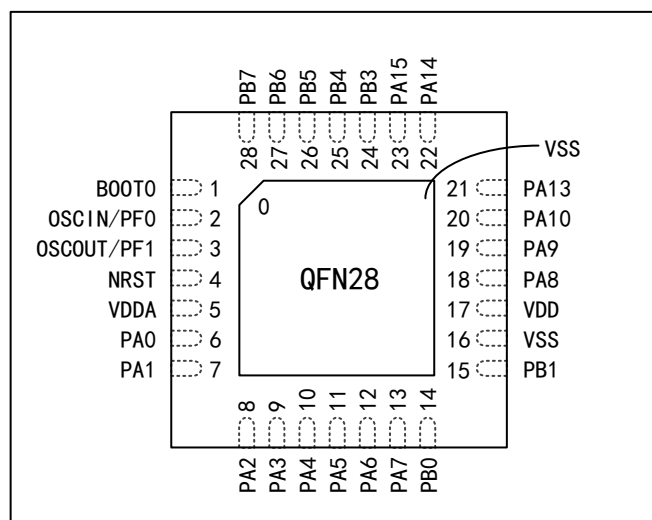
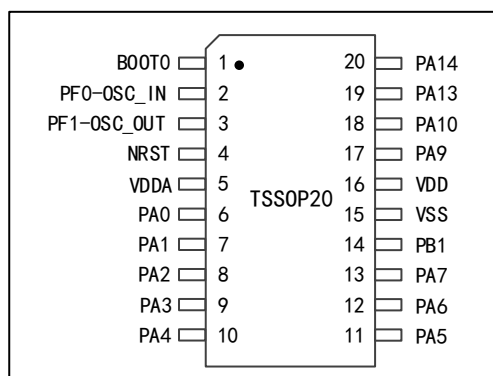


Figure 10 Pin configuration diagram of APM32F030x4x6x8 series TSSOP20



## 4.2. Pin function description

Table 14 Legend/abbreviation used in output pin table

| Name             | Abbreviations                                                                                                                              | Definition                                                  |
|------------------|--------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------|
| Pin name         | Unless otherwise specified in parentheses below the pin name, the pin functions during and after reset are the same as the actual pin name |                                                             |
| Pin type         | S                                                                                                                                          | Power supply pin                                            |
|                  | I                                                                                                                                          | Input pins only                                             |
|                  | I/O                                                                                                                                        | I/O pins                                                    |
| I/O structure    | FT                                                                                                                                         | I/O with 5V tolerance                                       |
|                  | FTf                                                                                                                                        | I/O with 5 V tolerance, FM+ function                        |
|                  | TTa                                                                                                                                        | I/O with 3.3 V tolerance is directly connected to ADC       |
|                  | TC                                                                                                                                         | Standard 3.3V I/O                                           |
|                  | B                                                                                                                                          | Dedicated BOOT0 pin                                         |
|                  | RST                                                                                                                                        | Bidirectional reset pin with built-in weak pull-up resistor |
| pay attention to | Unless otherwise specified in the notes, all I/O is set as floating input during and after reset                                           |                                                             |

|                 |                          |                                                                  |
|-----------------|--------------------------|------------------------------------------------------------------|
| Pin<br>function | Multiplexing<br>function | The function selected by GPIOx_AFR register                      |
|                 | Additional<br>function   | Functions directly selected/enabled through peripheral registers |

Table 15 Functional description of APM32F030x4x6x8 pin

| Pin name<br>(Function after<br>reset) | Pin coding |                  |        |       |       |         | Pin<br>Type | I/O<br>Structure | Notes | Pin function                                           |                                            |
|---------------------------------------|------------|------------------|--------|-------|-------|---------|-------------|------------------|-------|--------------------------------------------------------|--------------------------------------------|
|                                       | LQFP64     | LQFP48<br>/QFN48 | LQFP32 | QFN32 | QFN28 | TSSOP20 |             |                  |       | Multiplexing function                                  | Additional function                        |
| VDD                                   | 1          | 1                | -      | -     | -     | -       | S           | -                | -     | Complementary power supply                             |                                            |
| PC13                                  | 2          | 2                | -      | -     | -     | -       | I/O         | TC               | (1)   | -                                                      | RTC_TAMP1,<br>RTC_TS,<br>RTC_OUT,<br>WKUP2 |
| PC14-OSC32_IN<br>(PC14)               | 3          | 3                | -      | -     | -     | -       | I/O         | TC               | (1)   | -                                                      | OSC32_IN                                   |
| PC15-OSC32_OUT<br>(PC15)              | 4          | 4                | -      | -     | -     | -       | I/O         | TC               | (1)   | -                                                      | OSC32_OUT                                  |
| PF0-OSC_IN<br>(PF0)                   | 5          | 5                | 2      | 2     | 2     | 2       | I/O         | FT               | -     | -                                                      | OSC_IN                                     |
| PF1-OSC_OUT<br>(PF1)                  | 6          | 6                | 3      | 3     | 3     | 3       | I/O         | FT               | -     | -                                                      | OSC_OUT                                    |
| NRST                                  | 7          | 7                | 4      | 4     | 4     | 4       | I/O         | RST              | -     | Chip reset input/internal reset output<br>(active low) |                                            |
| PC0                                   | 8          | -                | -      | -     | -     | -       | I/O         | TTa              | -     | EVENTOUT                                               | ADC_IN10                                   |
| PC1                                   | 9          | -                | -      | -     | -     | -       | I/O         | TTa              | -     | EVENTOUT,                                              | ADC_IN11                                   |
| PC2                                   | 10         | -                | -      | -     | -     | -       | I/O         | TTa              | -     | EVENTOUT                                               | ADC_IN12                                   |
| PC3                                   | 11         | -                | -      | -     | -     | -       | I/O         | TTa              | -     | EVENTOUT                                               | ADC_IN13                                   |
| VSSA                                  | 12         | 8                | -      | 0     | -     | -       | S           | -                | -     | Analog ground                                          |                                            |
| VDDA                                  | 13         | 9                | 5      | 5     | 5     | 5       | S           | -                | -     | Analog power supply                                    |                                            |

| Pin name<br>(Function after reset) | Pin coding |               |        |       |       |         | Pin Type | I/O Structure | Notes | Pin function                                                    |                                 |
|------------------------------------|------------|---------------|--------|-------|-------|---------|----------|---------------|-------|-----------------------------------------------------------------|---------------------------------|
|                                    | LQFP64     | LQFP48 /QFN48 | LQFP32 | QFN32 | QFN28 | TSSOP20 |          |               |       | Multiplexing function                                           | Additional function             |
| PA0                                | 14         | 10            | 6      | 6     | 6     | 6       | I/O      | TTa           | -     | USART2_CTS                                                      | ADC_IN0,<br>RTC_TAMP2,<br>WKUP1 |
| PA1                                | 15         | 11            | 7      | 7     | 7     | 7       | I/O      | TTa           | -     | USART2_RTS,<br>EVENTOUT                                         | ADC_IN1                         |
| PA2                                | 16         | 12            | 8      | 8     | 8     | 8       | I/O      | TTa           | -     | USART2_TX,<br>TMR15_CH1                                         | ADC_IN2                         |
| PA3                                | 17         | 13            | 9      | 9     | 9     | 9       | I/O      | TTa           | -     | USART2_RX,<br>TMR15_CH2                                         | ADC_IN3                         |
| PF4                                | 18         | -             | -      | -     | -     | -       | I/O      | FT            | -     | EVENTOUT                                                        | -                               |
| PF5                                | 19         | -             | -      | -     | -     | -       | I/O      | FT            | -     | EVENTOUT                                                        | -                               |
| PA4                                | 20         | 14            | 10     | 10    | 10    | 10      | I/O      | TTa           | -     | SPI1_NSS,<br>USART2_CK,<br>TMR14_CH1                            | ADC_IN4                         |
| PA5                                | 21         | 15            | 11     | 11    | 11    | 11      | I/O      | TTa           | -     | SPI1_SCK                                                        | ADC_IN5                         |
| PA6                                | 22         | 16            | 12     | 12    | 12    | 12      | I/O      | TTa           | -     | SPI1_MISO,<br>TMR3_CH1,<br>TMR1_BKIN,<br>TMR16_CH1,<br>EVENTOUT | ADC_IN6                         |

| Pin name<br>(Function after<br>reset) | Pin coding |                  |        |       |       |         | Pin<br>Type | I/O<br>Structure | Notes | Pin function                                                                  |                     |
|---------------------------------------|------------|------------------|--------|-------|-------|---------|-------------|------------------|-------|-------------------------------------------------------------------------------|---------------------|
|                                       | LQFP64     | LQFP48<br>/QFN48 | LQFP32 | QFN32 | QFN28 | TSSOP20 |             |                  |       | Multiplexing function                                                         | Additional function |
| PA7                                   | 23         | 17               | 13     | 13    | 13    | 13      | I/O         | TTa              | -     | SPI1_MOSI,<br>TMR3_CH2,<br>TMR14_CH1,<br>TMR1_CH1N,<br>TMR17_CH1,<br>EVENTOUT | ADC_IN7             |
| PC4                                   | 24         | -                | -      | -     | -     | -       | I/O         | TTa              | -     | EVENTOUT                                                                      | ADC_IN14            |
| PC5                                   | 25         | -                | -      | -     | -     | -       | I/O         | TTa              | -     | -                                                                             | ADC_IN15            |
| PB0                                   | 26         | 18               | 14     | 14    | 14    | -       | I/O         | TTa              | -     | TMR3_CH3,<br>TMR1_CH2N,<br>EVENTOUT                                           | ADC_IN8             |
| PB1                                   | 27         | 19               | 15     | 15    | 15    | 14      | I/O         | TTa              | -     | TMR3_CH4,<br>TMR14_CH1,<br>TMR1_CH3N                                          | ADC_IN9             |
| PB2                                   | 28         | 20               | -      | 16    | -     | -       | I/O         | FT               | -     | -                                                                             | -                   |
| PB10                                  | 29         | 21               | -      | -     | -     | -       | I/O         | FT               | -     | I2C2_SCL                                                                      | -                   |
| PB11                                  | 30         | 22               | -      | -     | -     | -       | I/O         | FT               | -     | I2C2_SDA,<br>EVENTOUT                                                         | -                   |
| VSS                                   | 31         | 23               | 16     | 0     | 16    | -       | S           | -                | -     | ground                                                                        |                     |
| VDD                                   | 32         | 24               | 17     | 17    | 17    | 16      | S           | -                | -     | Digital power supply                                                          |                     |
| PB12                                  | 33         | 25               | -      | -     | -     | -       | I/O         | FT               | -     | SPI2_NSS,<br>TMR1_BKIN,<br>EVENTOUT                                           | -                   |

| Pin name<br>(Function after reset) | Pin coding |               |        |       |       |         | Pin Type | I/O Structure | Notes | Pin function                                         |                     |
|------------------------------------|------------|---------------|--------|-------|-------|---------|----------|---------------|-------|------------------------------------------------------|---------------------|
|                                    | LQFP64     | LQFP48 /QFN48 | LQFP32 | QFN32 | QFN28 | TSSOP20 |          |               |       | Multiplexing function                                | Additional function |
| PB13                               | 34         | 26            | -      | -     | -     | -       | I/O      | FT            | -     | SPI2_SCK,<br>TMR1_CH1N                               | -                   |
| PB14                               | 35         | 27            | -      | -     | -     | -       | I/O      | FT            | -     | SPI2_MISO,<br>TMR1_CH2N,<br>TMR15_CH1                | -                   |
| PB15                               | 36         | 28            | -      | -     | -     | -       | I/O      | FT            | -     | SPI2_MOSI,<br>TMR1_CH3N,<br>TMR15_CH1N,<br>TMR15_CH2 | RTC_REFIN           |
| PC6                                | 37         | -             | -      | -     | -     | -       | I/O      | FT            | -     | TMR3_CH1                                             | -                   |
| PC7                                | 38         | -             | -      | -     | -     | -       | I/O      | FT            | -     | TMR3_CH2                                             | -                   |
| PC8                                | 39         | -             | -      | -     | -     | --      | I/O      | FT            | -     | TMR3_CH3                                             | -                   |
| PC9                                | 40         | -             | -      | -     | -     | -       | I/O      | FT            | -     | TMR3_CH4                                             | -                   |
| PA8                                | 41         | 29            | 18     | 18    | 18    | -       | I/O      | FT            | -     | USART1_CK,<br>TMR1_CH1,<br>EVENTOUT,<br>MCO          | -                   |
| PA9                                | 42         | 30            | 19     | 19    | 19    | 17      | I/O      | FT            | -     | USART1_TX,<br>TMR1_CH2,<br>TMR15_BKIN                | -                   |
| PA10                               | 43         | 31            | 20     | 20    | 20    | 18      | I/O      | FT            | -     | USART1_RX,<br>TMR1_CH3,<br>TMR17_BKIN                | -                   |

| Pin name<br>(Function after<br>reset) | Pin coding |                  |        |       |       |         | Pin<br>Type | I/O<br>Structure | Notes | Pin function                         |                     |
|---------------------------------------|------------|------------------|--------|-------|-------|---------|-------------|------------------|-------|--------------------------------------|---------------------|
|                                       | LQFP64     | LQFP48<br>/QFN48 | LQFP32 | QFN32 | QFN28 | TSSOP20 |             |                  |       | Multiplexing function                | Additional function |
| PA11                                  | 44         | 32               | 21     | 21    | -     | -       | I/O         | FT               | -     | USART1_CTS,<br>TMR1_CH4,<br>EVENTOUT | -                   |
| PA12                                  | 45         | 33               | 22     | 22    | -     | -       | I/O         | FT               | -     | USART1_RTS,<br>TMR1_ETR,<br>EVENTOUT | -                   |
| PA13<br>(SWDIO)                       | 46         | 34               | 23     | 23    | 21    | 19      | I/O         | FT               | (2)   | IR_OUT,SWDIO                         | -                   |
| PF6                                   | 47         | 35               | -      | -     | -     | -       | I/O         | FT               | -     | I2C2_SCL                             | -                   |
| PF7                                   | 48         | 36               | -      | -     | -     | -       | I/O         | FT               | -     | I2C2_SDA                             | -                   |
| PA14<br>(SWCLK)                       | 49         | 37               | 24     | 24    | 22    | 20      | I/O         | FT               | (2)   | USART2_TX,<br>SWCLK                  | -                   |
| PA15                                  | 50         | 38               | 25     | 25    | 23    | -       | I/O         | FT               | -     | SPI1_NSS,<br>USART2_RX,<br>EVENTOUT  | -                   |
| PC10                                  | 51         | -                | -      | -     | -     | -       | I/O         | FT               | -     | -                                    | -                   |
| PC11                                  | 52         | -                | -      | -     | -     | -       | I/O         | FT               | -     | -                                    | -                   |
| PC12                                  | 53         | -                | -      | -     | -     | -       | I/O         | FT               | -     | -                                    | -                   |
| PD2                                   | 54         | -                | -      | -     | -     | -       | I/O         | FT               | -     | TMR3_ETR                             | -                   |
| PB3                                   | 55         | 39               | 26     | 26    | 24    | -       | I/O         | FT               | -     | SPI1_SCK,<br>EVENTOUT                | -                   |



| Pin name<br>(Function after<br>reset) | Pin coding |                  |        |       |       |         | Pin<br>Type | I/O<br>Structure | Notes | Pin function                                        |                     |
|---------------------------------------|------------|------------------|--------|-------|-------|---------|-------------|------------------|-------|-----------------------------------------------------|---------------------|
|                                       | LQFP64     | LQFP48<br>/QFN48 | LQFP32 | QFN32 | QFN28 | TSSOP20 |             |                  |       | Multiplexing function                               | Additional function |
| PB4                                   | 56         | 40               | 27     | 27    | 25    | -       | I/O         | FT               | -     | SPI1_MISO,<br>TMR3_CH1,<br>EVENTOUT                 | -                   |
| PB5                                   | 57         | 41               | 28     | 28    | 26    | -       | I/O         | FT               | -     | SPI1_MOSI,<br>I2C1_SMBA,<br>TMR16_BKIN,<br>TMR3_CH2 | -                   |
| PB6                                   | 58         | 42               | 29     | 29    | 27    | -       | I/O         | FT               | -     | I2C1_SCL,<br>USART1_TX,<br>TMR16_CH1N               | -                   |
| PB7                                   | 59         | 43               | 30     | 30    | 28    | -       | I/O         | FT               | -     | I2C1_SDA,<br>USART1_RX,<br>TMR17_CH1N               | -                   |
| BOOT0                                 | 60         | 44               | 31     | 31    | 1     | 1       | I           | B                | -     | Memory startup selection                            |                     |
| PB8                                   | 61         | 45               | -      | 32    | -     | -       | I/O         | FTf              | -     | I2C1_SCL,<br>TMR16_CH1                              | -                   |
| PB9                                   | 62         | 46               | -      | -     | -     | -       | I/O         | FTf              | -     | I2C1_SDA,<br>IR_OUT,<br>TMR17_CH1,<br>EVENTOUT      | -                   |
| VSS                                   | 63         | 47/0             | 32     | 0     | 0     | 15      | S           | -                | -     | ground                                              |                     |
| VDD                                   | 64         | 48               | 1      | 1     | -     | 16      | S           | -                | -     | Digital power supply                                |                     |

**Note:**

- (1) If PF0 and PF1 need to be configured as GPIO, HSEEN must be disabled first.
- (2) PC13, PC14 and PC15 are powered by the power switch. Because the switch only absorbs limited current (3 mA), the use of PC13 to PC15 of GPIO is limited in output mode: when the large load is 30 pF, the speed should not exceed 2 MHz; It is not used as a current source (for example, driving light emitting diodes).
- (3) Upon reset, these pins are configured as SWDIO and SWCLK multiplexing functions, and the internal pull-up of SWDIO pin and the internal pull-down of SWCLK pin are activated.

**Table 16 Select multiplexing function for port A through GPIOA\_AFR register**

| Pin name | AF0        | AF1        | AF2       | AF3      | AF4       | AF5       | AF6      |
|----------|------------|------------|-----------|----------|-----------|-----------|----------|
| PA0      | -          | USART2_CTS | -         | -        |           | -         | -        |
| PA1      | EVENTOUT   | USART2_RTS | -         | -        |           |           | -        |
| PA2      | TMR15_CH1  | USART2_TX  | -         | -        | -         | -         | -        |
| PA3      | TMR15_CH2  | USART2_RX  | -         | -        | -         | -         | -        |
| PA4      | SPI1_NSS   | USART2_CK  | -         | -        | TMR14_CH1 |           | -        |
| PA5      | SPI1_SCK   | -          | -         | -        | -         |           | -        |
| PA6      | SPI1_MISO  | TMR3_CH1   | TMR1_BKIN | -        |           | TMR16_CH1 | EVENTOUT |
| PA7      | SPI1_MOSI  | TMR3_CH2   | TMR1_CH1N | -        | TMR14_CH1 | TMR17_CH1 | EVENTOUT |
| PA8      | MCO        | USART1_CK  | TMR1_CH1  | EVENTOUT | -         | -         | -        |
| PA9      | TMR15_BKIN | USART1_TX  | TMR1_CH2  | -        |           |           | -        |
| PA10     | TMR17_BKIN | USART1_RX  | TMR1_CH3  | -        |           | -         | -        |
| PA11     | EVENTOUT   | USART1_CTS | TMR1_CH4  | -        | -         | SCL       | -        |
| PA12     | EVENTOUT   | USART1_RTS | TMR1_ETR  | -        | -         | SDA       | -        |
| PA13     | SWDIO      | IR_OUT     | -         | -        | -         | -         | -        |
| PA14     | SWCLK      | USART2_TX  | -         | -        | -         | -         | -        |
| PA15     | SPI1_NSS   | USART2_RX  | -         | EVENTOUT |           | -         | -        |

**Table 17 Select multiplexing function for port B through GPIOB\_AFR register**

| Pin name | AF0       | AF1       | AF2        | AF3        | AF4 | AF5        |
|----------|-----------|-----------|------------|------------|-----|------------|
| PB0      | EVENTOUT  | TMR3_CH3  | TMR1_CH2N  | -          |     | -          |
| PB1      | TMR14_CH1 | TMR3_CH4  | TMR1_CH3N  | -          |     | -          |
| PB2      | -         | -         | -          | -          | -   | -          |
| PB3      | SPI1_SCK  | EVENTOUT  | -          | -          |     | -          |
| PB4      | SPI1_MISO | TMR3_CH1  | EVENTOUT   | -          |     | TMR17_BKIN |
| PB5      | SPI1_MOSI | TMR3_CH2  | TMR16_BKIN | -          |     | -          |
| PB6      | USART1_TX | I2C1_SCL  | TMR16_CH1N | -          | -   | -          |
| PB7      | USART1_RX | I2C1_SDA  | TMR17_CH1N | -          |     | -          |
| PB8      | -         | I2C1_SCL  | TMR16_CH1  | -          | -   | -          |
| PB9      | IR_OUT    | I2C1_SDA  | TMR17_CH1  | EVENTOUT   | -   | -          |
| PB10     | -         | I2C2_SCL  | -          | -          |     | -          |
| PB11     | EVENTOUT  | I2C2_SDA  | -          | -          |     | -          |
| PB12     | SPI2_NSS  | EVENTOUT  | TMR1_BKIN  | -          |     | -          |
| PB13     | SPI2_SCK  | -         | TMR1_CH1N  | -          |     |            |
| PB14     | SPI2_MISO | TMR15_CH1 | TMR1_CH2N  | -          |     |            |
| PB15     | SPI2_MOSI | TMR15_CH2 | TMR1_CH3N  | TMR15_CH1N | -   | -          |

Table 18 **Select multiplexing function for port C through GPIOC\_AFR register**

| Pin name | AF0      |
|----------|----------|
| PC0      | EVENTOUT |
| PC1      | EVENTOUT |
| PC2      | EVENTOUT |
| PC3      | EVENTOUT |
| PC4      | EVENTOUT |
| PC5      | -        |
| PC6      | TMR3_CH1 |
| PC7      | TMR3_CH2 |
| PC8      | TMR3_CH3 |
| PC9      | TMR3_CH4 |
| PC10     |          |
| PC11     |          |
| PC12     |          |
| PC13     | -        |
| PC14     | -        |
| PC15     | -        |

Table 19 **Select multiplexing function for port D through GPIOD\_AFR register**

| Pin name | AF0      |
|----------|----------|
| PD2      | TMR3_ETR |

Table 20 **Select multiplexing function for port F through GPIOF\_AFR register**

| Pin name | AF0 |
|----------|-----|
| PF0      | -   |
| PF1      | -   |

## 5. Electrical specification

### 5.1. Test condition

All voltage parameters (unless otherwise specified) refer to  $V_{SS}$ .

#### 5.1.1 Maximum and minimum value

Unless otherwise specified, all products are tested on the production line at  $T_A=25^{\circ}\text{C}$ . Its maximum and minimum values can support the worst environmental temperature, power supply voltage and clock frequency.

In the notes at the bottom of each table, it is stated that the data obtained through comprehensive evaluation, design simulation or process characteristics are not tested on the production line; On the basis of comprehensive evaluation, after passing the sample test, take the average value and add and subtract three times the standard deviation (average  $\pm 3\Sigma$ ) to get the maximum and minimum values.

#### 5.1.2 Typical value

Unless otherwise specified, typical data are based on  $T_A=25^{\circ}\text{C}$  and  $V_{DD}=V_{DDA}=3.3\text{V}$ ; These data are for design guidance only.

#### 5.1.3 Typical curve

Unless otherwise specified, typical curves will not be tested on the production line, and will only be used for design guidance.

#### 5.1.4 Load capacitance

Figure 11 Load conditions when measuring pin parameters

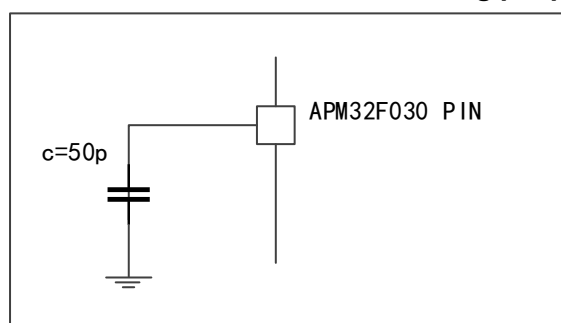


Figure 12 Pin input voltage measurement scheme

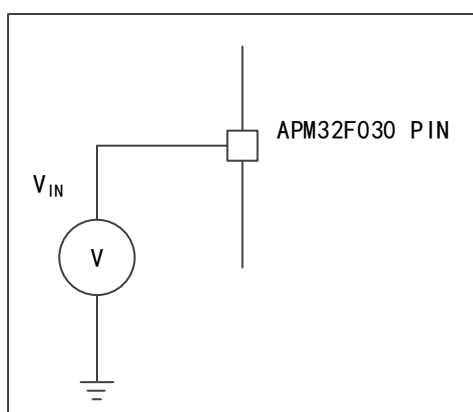
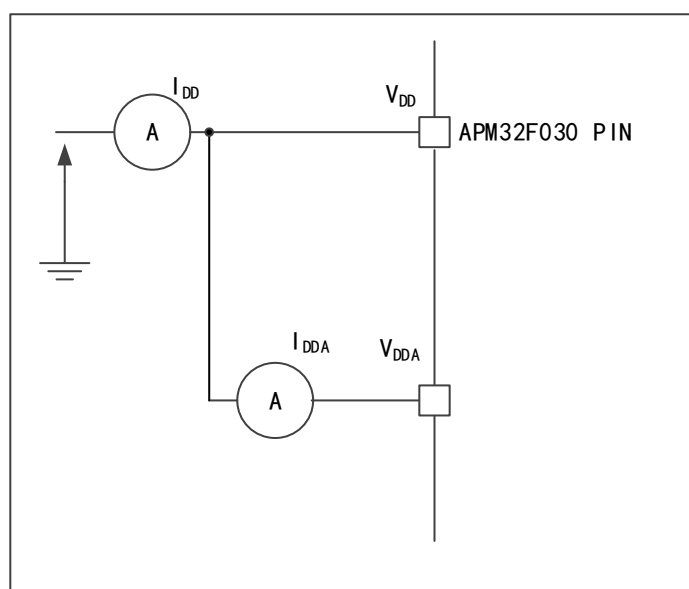


Figure 13 Current consumption measurement scheme



## 5.2. Absolute maximum rating

If the load on the device exceeds the absolute maximum rating, it may cause permanent damage to the device. Only the maximum load that can be borne is given here, and there is no guarantee that the device functions normally under this condition.

### 5.2.1 Maximum rated voltage characteristics

Table 21 Maximum rated voltage characteristics

| Symbol                  | description                                              | Minimum value | Maximum value | Unit |
|-------------------------|----------------------------------------------------------|---------------|---------------|------|
| $V_{DD}-V_{SS}$         | External main supply voltage ( $V_{DD}$ ) <sup>(1)</sup> | -0.3          | 4.0           | V    |
|                         | External analog supply voltage ( $V_{DDA}$ )             | -0.3          | 4.0           |      |
| $V_{DD}-V_{DDA}$        | Voltage difference allowed by $V_{DD}>V_{DDA}$           | -             | 0.4           |      |
| $V_{IN}$ <sup>(2)</sup> | Input voltage on FT and FTf pins <sup>(2)</sup>          | $V_{SS}-0.3$  | $V_{DD}+4.0$  |      |
|                         | Input voltage on TTA pin <sup>(2)</sup>                  | $V_{SS}-0.3$  | 4.0           |      |
|                         | BOOT0                                                    | 0             | $V_{DD}+4.0$  |      |
|                         | Input voltage on any other pin                           | $V_{SS}-0.3$  | 4.0           |      |
| $ \Delta V_{DDx} $      | Voltage difference between different power supply pins   | -             | 50            | mV   |
| $ V_{SSx}-V_{SS} $      | Voltage difference between different grounding pins      | -             | 50            |      |

**Note:**

- (1) All power supply ( $V_{DD}$ ,  $V_{DDA}$ ) and ground ( $V_{SS}$ ,  $V_{SSA}$ ) pins must always be connected to the power supply within the external limited range.
- (2) If  $V_{IN}$  is within the maximum range,  $I_{IN(PIN)}$  will not exceed its limit. If  $V_{IN}$  exceeds the maximum value, the value of  $I_{IN(PIN)}$  must be externally limited to ensure that its maximum value is not exceeded. The forward injection current appears when  $V_{IN}$  is greater than  $V_{DD}$ , while the reverse injection current appears when  $V_{IN}$  is less than  $V_{SS}$ .

### 5.2.2 Maximum Rated Current Features

Table 22 Maximum Rated Current Features

| Symbol           | Description                                                                 | Maximum | Unit |
|------------------|-----------------------------------------------------------------------------|---------|------|
| $\Sigma I_{VDD}$ | Total current into sum of all $V_{DD}$ power lines (source) <sup>(1)</sup>  | 120     | mA   |
| $\Sigma I_{VSS}$ | Total current out of sum of all $V_{SS}$ ground lines (sink) <sup>(1)</sup> | -120    |      |
| $I_{VDD(PIN)}$   | Maximum current into each $V_{DD}$ power pin (source) <sup>(1)</sup>        | 100     |      |
| $I_{VSS(PIN)}$   | Maximum current out of each $V_{SS}$ ground pin (sink) <sup>(1)</sup>       | -100    |      |
| $I_{IO(PIN)}$    | Output current sunk by any I/O and control pin                              | 25      |      |

|                             |                                                                                 |                      |  |
|-----------------------------|---------------------------------------------------------------------------------|----------------------|--|
|                             | Output current source by any I/O and control pin                                | -25                  |  |
| $\Sigma I_{IO(PIN)}$        | Total output current sunk by sum of all I/Os and control pins <sup>(2)</sup>    | 80                   |  |
|                             | Total output current sourced by sum of all I/Os and control pins <sup>(2)</sup> | -80                  |  |
| $I_{INJ(PIN)}^{(3)}$        | Injected current on FT and FTf pins                                             | -5/+0 <sup>(4)</sup> |  |
|                             | Injected current on TC and RST pins                                             | $\pm 5$              |  |
|                             | Injected current on TTa pins <sup>(5)</sup>                                     | $\pm 5$              |  |
| $\Sigma I_{INJ(PIN)}^{(2)}$ | Total injected current (sum of all I/O and control pins) <sup>(6)</sup>         | $\pm 25$             |  |

**Note:**

- (1) All power ( $V_{DD}$ ,  $V_{DDA}$ ) and ground ( $V_{SS}$ ,  $V_{SSA}$ ) pins must always be connected to a power supply within the external allowable range.
- (2) If  $V_{IN}$  does not exceed the maximum value,  $I_{INJ(PIN)}$  will not exceed its limit. If  $V_{IN}$  exceeds the maximum value,  $I_{INJ(PIN)}$  must be externally limited to not exceed its maximum value. When  $V_{IN} > V_{DD}$ , there is a forward injection current; when  $V_{IN} < V_{SS}$ , there is a reverse injection current.
- (3) Reverse injection current can interfere with the analog performance of the ADC.
- (4) When several I/O ports have injection current at the same Time, the maximum value of  $\Sigma I_{INJ(PIN)}$  is the sum of the instantaneous absolute values of the forward injection current and the reverse injection current. These results are based on the calculation of the maximum value of  $\Sigma I_{INJ(PIN)}$  on the four I/O port pins of the device.
- (5) On these I/Os, a positive injection is induced by  $V_{IN} > V_{DDA}$ . Negative injection disturbs the analog performance of the device.
- (6) When several inputs are submitted to a current injection, the maximum  $\Sigma I_{INJ(PIN)}$  is the absolute sum of the positive and negative injected currents (instantaneous values).

### 5.2.3 Maximum electrostatic characteristics

Table 23      **Electrostatic discharge (ESD)**



| Symbol         | Parameter                                                  | Condition                 | Maximum value | Unit |
|----------------|------------------------------------------------------------|---------------------------|---------------|------|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (manikin)                  | $T_A=+25^{\circ}\text{C}$ | 3000          | V    |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charging equipment model) | $T_A=+25^{\circ}\text{C}$ | 2000          |      |

**Note:** The samples are measured by a third-party testing organization and are not tested in production.

#### 5.2.4 Static latch

Table 24 Static latch

| Symbol | Parameter          | Condition                                     | Type       |
|--------|--------------------|-----------------------------------------------|------------|
| LU     | Static latch class | $T_A=+25^{\circ}\text{C}/105^{\circ}\text{C}$ | class II A |

#### 5.2.5 Maximum temperature characteristics

Table 25 Temperature characteristics

| Symbol    | description                  | Numerical value | Unit               |
|-----------|------------------------------|-----------------|--------------------|
| $T_{STG}$ | Storage temperature range    | $-65 \sim +150$ | $^{\circ}\text{C}$ |
| $T_J$     | Maximum junction temperature | 150             | $^{\circ}\text{C}$ |

### 5.3. Testing under general working conditions

Table 26 General working conditions

| Symbol     | Parameter                        | Condition                                | Minimum value | Maximum value | Unit |
|------------|----------------------------------|------------------------------------------|---------------|---------------|------|
| $F_{HCLK}$ | Internal AHB clock frequency     | -                                        | 0             | 48            | MHz  |
| $f_{PCLK}$ | Internal APB clock frequency     | -                                        | 0             | 48            |      |
| $V_{DD}$   | Standard operating voltage       | -                                        | 2             | 3.6           | V    |
| $V_{DDA}$  | Analog partial operating voltage | $V_{DDA}$ must not be less than $V_{DD}$ | 2.4           | 3.6           | V    |
| $V_{IN}$   | I/O input voltage                | TC and RST I/O                           | -0.3          | $V_{DD}+0.3$  | V    |
|            |                                  | TTa I/O                                  | -0.3          | $V_{DDA}+0.3$ |      |
|            |                                  | FT and FTf I/O                           | -0.3          | 5.5           |      |
|            |                                  | BOOT0                                    | 0             | 5.5           |      |

#### 5.3.1 Embedded reset and power control module characteristic test

The parameters given in Table 27 are derived from the test results under the

conditions of ambient temperature and power supply voltage summarized in Table 26.

**Table 27 Embedded reset and power control module features**

| Symbol               | Parameter                           | Condition                   | Minimum value | Typical value | Maximum value | Unit |
|----------------------|-------------------------------------|-----------------------------|---------------|---------------|---------------|------|
| $V_{POR/PDR}^{(1)}$  | Power-on/power-down reset threshold | Falling edge <sup>(2)</sup> | -             | 1.87          | -             | V    |
|                      |                                     | Rising edge                 | -             | 1.92          | -             | V    |
| $V_{PDRhyst}^{(3)}$  | PDR hysteresis                      | -                           | -             | 50            | -             | mV   |
| $T_{RSTTEMPO}^{(3)}$ | Reset duration                      | -                           | 1.70          | 2.51          | 3.32          | ms   |

**Note:**

- (1) PDR detector monitors  $V_{DD}$  and  $V_{DDA}$  (if enabled in option byte), POR detector monitors  $V_{DD}$  only.
- (2) Product characteristics are guaranteed by design to the minimum  $V_{POR/PDR}$  value
- (3) Guaranteed by design and not tested in production.

### 5.3.2 Built-in reference voltage characteristic test

The parameters given in Table 28 are derived from the test results under the conditions of ambient temperature and power supply voltage summarized in Table 26.

**Table 28 Built-in reference voltage**

| Symbol              | Parameter                                                        | Condition                                          | Minimum value | Typical value | Maximum value | Unit          |
|---------------------|------------------------------------------------------------------|----------------------------------------------------|---------------|---------------|---------------|---------------|
| $V_{REFINT}$        | Built-in reference voltage                                       | $-40^{\circ}\text{C} < T_A < +105^{\circ}\text{C}$ | 1.19          | 1.23          | 1.24          | V             |
| $t_{START}$         | ADC_IN17 buffer startup time                                     | -                                                  | -             | -             | 10            | $\mu\text{s}$ |
| $T_{S\_vrefint}$    | Sampling time of ADC when reading out internal reference voltage | -                                                  | 4             | -             | -             | $\mu\text{s}$ |
| $\Delta V_{REFINT}$ | Built-in reference voltage extends to temperature range          | $V_{DDA}=3.3\text{V}$                              | -             | -             | 10            | mV            |

### 5.3.3 Power consumption

Power consumption test environment:

- (1) Execute Dhrystone2.1, the compiling environment is KeilV5 and the compiling optimization level is L0.

- (2) All I/O pins are configured as analog inputs and are connected to a static level of  $V_{DD}$  or  $V_{SS}$  (non-loaded).
- (3) Unless otherwise specified, all peripherals are turned off.
- (4) The relationship between Flash waiting period setting and  $f_{HCMU}$ :  
0~24MHz—0 waiting period, 24~48MHz—1 waiting period.
- (5) When it is greater than 24MHz, the instruction prefetch function is enabled  
(Note: this bit must be set before clock setting and bus frequency division).
- (6) When the peripheral is turned on:  $f_{PCLK}=f_{HCLK}$ .

**Table 29 The program is executed in Flash, and the running mode consumes power**

| Parameter    | Condition                                                | $f_{HCMU}$ | Typical value <sup>(1)</sup>                    |                     | Maximum value <sup>(1)</sup>                     |                     |
|--------------|----------------------------------------------------------|------------|-------------------------------------------------|---------------------|--------------------------------------------------|---------------------|
|              |                                                          |            | $T_A=25^{\circ}\text{C}$ , $V_{DD}=3.3\text{V}$ |                     | $T_A=105^{\circ}\text{C}$ , $V_{DD}=3.6\text{V}$ |                     |
|              |                                                          |            | $I_{DDA}(\mu\text{A})$                          | $I_{DD}(\text{mA})$ | $I_{DDA}(\mu\text{A})$                           | $I_{DD}(\text{mA})$ |
| Running mode | External clock <sup>(2)</sup> , enabling all peripherals | 48MHz      | 105.69                                          | 10.0                | 125.76                                           | 10.39               |
|              |                                                          | 24MHz      | 59.64                                           | 5.67                | 74.78                                            | 5.88                |
|              |                                                          | 8MHz       | 1.44                                            | 2.31                | 7.7                                              | 2.43                |
|              | External clock <sup>(2)</sup> , turn off all peripherals | 48MHz      | 105.73                                          | 6.94                | 125.99                                           | 7.18                |
|              |                                                          | 24MHz      | 59.7                                            | 4.17                | 75.09                                            | 4.29                |
|              |                                                          | 8MHz       | 3.3                                             | 1.80                | 7.15                                             | 1.90                |
|              | Internal clock to enable all peripherals                 | 48MHz      | 178.5                                           | 9.6                 | 198.3                                            | 10.04               |
|              |                                                          | 24MHz      | 136.8                                           | 5.24                | 153.3                                            | 5.45                |
|              |                                                          | 8MHz       | 81.4                                            | 1.88                | 91.7                                             | 1.97                |
|              | Internal clock, turn off all peripherals                 | 48MHz      | 178.4                                           | 6.51                | 198.1                                            | 6.82                |
|              |                                                          | 24MHz      | 136.8                                           | 3.66                | 153.1                                            | 3.85                |
|              |                                                          | 8MHz       | 81.4                                            | 1.33                | 91.7                                             | 1.40                |

**Note:**

- (1) Data based on comprehensive evaluation will not be tested in production unless otherwise specified.
- (2) The external clock is 8MHz. when  $f_{HCMU}>8\text{MHz}$ , PLL is started.

**Table 30 The program is executed in SRAM, and the running mode consumes power**

| Parameter    | Condition                                                | $f_{HCMU}$ | Typical value <sup>(1)</sup>                    |                     | Maximum value <sup>(1)</sup>                     |                     |
|--------------|----------------------------------------------------------|------------|-------------------------------------------------|---------------------|--------------------------------------------------|---------------------|
|              |                                                          |            | $T_A=25^{\circ}\text{C}$ , $V_{DD}=3.3\text{V}$ |                     | $T_A=105^{\circ}\text{C}$ , $V_{DD}=3.6\text{V}$ |                     |
|              |                                                          |            | $I_{DDA}(\mu\text{A})$                          | $I_{DD}(\text{mA})$ | $I_{DDA}(\mu\text{A})$                           | $I_{DD}(\text{mA})$ |
| Running mode | External clock <sup>(2)</sup> , enabling all peripherals | 48MHz      | 105.73                                          | 7.48                | 125.63                                           | 8.0                 |
|              |                                                          | 24MHz      | 59.67                                           | 4.1                 | 74.76                                            | 4.7                 |

| Parameter | Condition                                                | f <sub>HCMU</sub> | Typical value <sup>(1)</sup>                   |                      | Maximum value <sup>(1)</sup>                    |                      |
|-----------|----------------------------------------------------------|-------------------|------------------------------------------------|----------------------|-------------------------------------------------|----------------------|
|           |                                                          |                   | T <sub>A</sub> =25°C,<br>V <sub>DD</sub> =3.3V |                      | T <sub>A</sub> =105°C,<br>V <sub>DD</sub> =3.6V |                      |
|           |                                                          |                   | I <sub>DDA</sub> (μA)                          | I <sub>DD</sub> (mA) | I <sub>DDA</sub> (μA)                           | I <sub>DD</sub> (mA) |
|           | External clock <sup>(2)</sup> , turn off all peripherals | 8MHz              | 3.3                                            | 1.9                  | 7.20                                            | 2.2                  |
|           |                                                          | 48MHz             | 105.78                                         | 4.4                  | 125.98                                          | 4.60                 |
|           |                                                          | 24MHz             | 59.71                                          | 2.6                  | 74.96                                           | 2.7                  |
|           | Internal clock to enable all peripherals                 | 8MHz              | 3.3                                            | 1.4                  | 7.11                                            | 1.5                  |
|           |                                                          | 48MHz             | 178.5                                          | 7.06                 | 198.2                                           | 7.39                 |
|           |                                                          | 24MHz             | 139.8                                          | 3.65                 | 153.3                                           | 4.0                  |
|           | Internal clock, turn off all peripherals                 | 8MHz              | 81.4                                           | 1.37                 | 91.7                                            | 1.43                 |
|           |                                                          | 48MHz             | 178.5                                          | 3.94                 | 198.1                                           | 4.14                 |
|           |                                                          | 24MHz             | 136.8                                          | 2.07                 | 153.2                                           | 2.23                 |
|           |                                                          | 8MHz              | 81.4                                           | 0.79                 | 91.7                                            | 0.86                 |
|           |                                                          |                   |                                                |                      |                                                 |                      |
|           |                                                          |                   |                                                |                      |                                                 |                      |

**Note:**

- (1) According to the comprehensive evaluation, it is not tested in production.  
(2) The external clock is 8MHz. when f<sub>HCMU</sub>>8MHz, PLL is started.

**Table 31 Program is executed in SRAM or Flash, power consumption in sleep mode**

| Parameter  | Condition                                                | f <sub>HCMU</sub> | Typical value <sup>(1)</sup>                   |                      | Maximum value <sup>(1)</sup>                    |                      |
|------------|----------------------------------------------------------|-------------------|------------------------------------------------|----------------------|-------------------------------------------------|----------------------|
|            |                                                          |                   | T <sub>A</sub> =25°C,<br>V <sub>DD</sub> =3.3V |                      | T <sub>A</sub> =105°C,<br>V <sub>DD</sub> =3.6V |                      |
|            |                                                          |                   | I <sub>DDA</sub> (μA)                          | I <sub>DD</sub> (mA) | I <sub>DDA</sub> (μA)                           | I <sub>DD</sub> (mA) |
| Sleep mode | External clock <sup>(2)</sup> , enabling all peripherals | 48MHz             | 105.77                                         | 5.41                 | 125.88                                          | 5.54                 |
|            |                                                          | 24MHz             | 59.70                                          | 3.03                 | 74.91                                           | 3.16                 |
|            |                                                          | 8MHz              | 1.45                                           | 1.42                 | 7.12                                            | 1.50                 |
|            | External clock <sup>(2)</sup> , turn off all peripherals | 48MHz             | 105.86                                         | 2.0                  | 125.9                                           | 2.13                 |
|            |                                                          | 24MHz             | 59.8                                           | 1.35                 | 75.08                                           | 1.47                 |
|            |                                                          | 8MHz              | 1.44                                           | 0.84                 | 7.14                                            | 0.94                 |
|            | Internal clock to enable all peripherals                 | 48MHz             | 161.55                                         | 4.93                 | 187.25                                          | 5.14                 |
|            |                                                          | 24MHz             | 115.48                                         | 2.60                 | 136.87                                          | 2.72                 |
|            |                                                          | 8MHz              | 58.0                                           | 0.99                 | 72.41                                           | 1.05                 |
|            | Internal clock, turn off all peripherals                 | 48MHz             | 161.71                                         | 1.52                 | 187.85                                          | 1.69                 |
|            |                                                          | 24MHz             | 115.54                                         | 0.86                 | 137.13                                          | 0.99                 |
|            |                                                          | 8MHz              | 58.0                                           | 0.37                 | 72.35                                           | 0.46                 |

**Note:**

- (1) According to the comprehensive evaluation, it is not tested in production.  
(2) The external clock is 8MHz. when f<sub>HCMU</sub>>8MHz, PLL is started.

**Table 32 Power consumption in halt and standby mode**

| Parameter    | Condition                             |                                                                                                                                                     | Typical value<br>(T <sub>A</sub> =25°C) |                         |                          |                         | Maximum value <sup>(1)</sup><br>(T <sub>A</sub> =105°C) |                         |
|--------------|---------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------|-------------------------|--------------------------|-------------------------|---------------------------------------------------------|-------------------------|
|              |                                       |                                                                                                                                                     | V <sub>DD</sub> =2.4 V                  |                         | V <sub>DD</sub> = 3.3V   |                         | V <sub>DD</sub> =3.6 V                                  |                         |
|              |                                       |                                                                                                                                                     | I <sub>DDA</sub><br>(μA)                | I <sub>DD</sub><br>(μA) | I <sub>DDA</sub><br>(μA) | I <sub>DD</sub><br>(μA) | I <sub>DDA</sub><br>(μA)                                | I <sub>DD</sub><br>(μA) |
| halt mode    | V <sub>DDA</sub><br>monitoring<br>ON  | The voltage regulator is in running mode, and the low-speed and high-speed internal RC oscillators and high-speed oscillators are off               | 2.43                                    | 21.1                    | 2.98                     | 21.9                    | 7.0                                                     | 62.6                    |
|              |                                       | The voltage regulator is in low power consumption mode, and the low-speed and high-speed internal RC oscillators and high-speed oscillators are off | 2.43                                    | 6.47                    | 2.98                     | 7.42                    | 7.0                                                     | 44.9                    |
| Standby mode |                                       | Low-speed internal RC oscillator and independent watchdog are on                                                                                    | 2.62                                    | 2.42                    | 3.33                     | 3.72                    | 6.63                                                    | 22.2                    |
|              |                                       | The low-speed internal RC oscillator and the independent watchdog are off                                                                           | 2.28                                    | 1.96                    | 2.83                     | 3.08                    | 6.11                                                    | 21.5                    |
| halt mode    | V <sub>DDA</sub><br>monitoring<br>OFF | The voltage regulator is in run mode, and the low-speed and high-speed internal RC oscillators and high-speed oscillators are off                   | 1.3                                     | 17.7                    | 1.5                      | 18.0                    | 3.4                                                     | 56.4                    |
|              |                                       | The voltage regulator is in low power consumption mode, and the low-speed and high-speed internal RC oscillators and high-speed oscillators are off | 1.3                                     | 6.33                    | 1.5                      | 7.38                    | 3.3                                                     | 44.9                    |
| Standby mode |                                       | Low-speed internal RC oscillator and independent watchdog are on                                                                                    | 1.6                                     | 2.36                    | 1.9                      | 3.7                     | 3.8                                                     | 22.2                    |
|              |                                       | The low-speed internal RC oscillator and the independent watchdog are off                                                                           | 1.2                                     | 1.93                    | 1.31                     | 3.05                    | 3.0                                                     | 21.5                    |

**Note: According to the comprehensive evaluation, it is not tested in production.**

### 5.3.4 External clock source characteristics

#### High Speed External Clock Generated by Crystal Resonator (HSECLK osc)

For detailed parameters (frequency, package, precision, etc.) of crystal resonator, please consult the corresponding manufacturer.

Table 33 Characteristics of HSECLK 4~32MHz Oscillator <sup>(1)</sup>

| Symbol           | Parameter                  | Condition                                                                              | Minimum value | Typical value | Maximum value | Unit          |
|------------------|----------------------------|----------------------------------------------------------------------------------------|---------------|---------------|---------------|---------------|
| $f_{OSC\_IN}$    | Oscillator frequency       | -                                                                                      | 4             | 8             | 32            | MHz           |
| $R_F$            | Feedback resistance        | -                                                                                      | -             | 200           | -             | k $\Omega$    |
| $I_{DD}$         | HSECLK current consumption | $V_{DD} = 3.3\text{ V}$ ,<br>$R_m = 45\ \Omega$ ,<br>$C_L = 10\text{ pF}@8\text{ MHz}$ | -             | 660           | -             | $\mu\text{A}$ |
| $t_{SU(HSECLK)}$ | Startup time               | $V_{DD}$ is stable                                                                     |               | 1.7           |               | ms            |

**Note:** It is guaranteed by design and has not been tested in production.

#### Low Speed External Clock (LSECLK osc) Generated by Crystal Resonator

For detailed parameters (frequency, package, precision, etc.) of crystal resonator, please consult the corresponding manufacturer.

Table 34 LSECLK oscillator characteristics ( $f_{LSECLK}=32.768\text{KHz}$ ) <sup>(1)</sup>

| Symbol                 | Parameter                  | Condition             | Minimum value | Typical value | Maximum value | Unit          |
|------------------------|----------------------------|-----------------------|---------------|---------------|---------------|---------------|
| $I_{DD}$               | LSECLK current consumption | High driving ability  |               | 1.5           |               | $\mu\text{A}$ |
| $t_{SU(LSECLK)}^{(2)}$ | Startup time               | $V_{DDIOX}$ is stable | -             | 2             | -             | s             |

**Note:**

- (1) Guaranteed by design and not tested in production.
- (2)  $t_{SU(LSECLK)}$  is the starting time, which is measured from the time when LSECLK is enabled by software to the time when stable oscillation at 32.768KHz is obtained. This value is measured using a standard crystal resonator, which may vary greatly due to different crystal manufacturers.

### 5.3.5 Internal clock source characteristics

#### Test of high speed internal (HSICLK)RC oscillator

Table 35 HSICLK oscillator characteristics

| Symbol       | Parameter | Condition | Minimum value | Typical value | Maximum value | Unit |
|--------------|-----------|-----------|---------------|---------------|---------------|------|
| $f_{HSICLK}$ | Frequency | -         | -             | 8             | -             | MHz  |

| Symbol                    | Parameter                           | Condition                                          |                                                   | Minimum value | Typical value | Maximum value | Unit |
|---------------------------|-------------------------------------|----------------------------------------------------|---------------------------------------------------|---------------|---------------|---------------|------|
| A <sub>CCHSICKL</sub>     | Accuracy of HSICLK oscillator       | Factory calibration                                | V <sub>DD</sub> =3.3V<br>T <sub>A</sub> =25°C     | -1            | -             | 1             | %    |
|                           |                                     |                                                    | V <sub>DD</sub> =2-3.6V T <sub>A</sub> =-40~105°C | -5            | -             | 5             | %    |
| t <sub>SU</sub> (HSICLK)  | HSICLK oscillator start-up time     | V <sub>DD</sub> =3.3V<br>T <sub>A</sub> =-40~105°C |                                                   | -             | -             | 2             | μs   |
| I <sub>DDA</sub> (HSICLK) | HSICLK oscillator power consumption | -                                                  |                                                   | -             | 60            | -             | μA   |

**Note:** According to the comprehensive evaluation, it is not tested in production.

**Table 36 Characteristics of HSICLK14 oscillator**

| Symbol                      | Parameter                                | Condition                                          |                                                   | Minimum value | Typical value | Maximum value | Unit |
|-----------------------------|------------------------------------------|----------------------------------------------------|---------------------------------------------------|---------------|---------------|---------------|------|
| f <sub>HSICLK14</sub>       | Frequency                                | -                                                  |                                                   | -             | 14            | -             | MHz  |
| A <sub>CCHSICKL14</sub>     | Accuracy of HSICLK14 oscillator          | Factory calibration                                | V <sub>DD</sub> =3.3V<br>T <sub>A</sub> =25°C     | -1            | -             | 1             | %    |
|                             |                                          |                                                    | V <sub>DD</sub> =2-3.6V T <sub>A</sub> =-40~105°C | -5            | -             | 5             | %    |
| t <sub>SU</sub> (HSICLK14)  | Starting time of HSICLK14 oscillator     | V <sub>DD</sub> =3.3V<br>T <sub>A</sub> =-40~105°C |                                                   | -             | -             | 2             | μs   |
| I <sub>DDA</sub> (HSICLK14) | Power consumption of HSICLK14 oscillator | -                                                  |                                                   | -             | 72            | -             | μA   |

**Note:** According to the comprehensive evaluation, it is not tested in production.

### Low speed internal (LSICLK)RC oscillator test

**Table 37 LSICLK oscillator characteristics**

| Symbol                   | Parameter                                                                               | Minimum value | Typical value | Maximum value | Unit |
|--------------------------|-----------------------------------------------------------------------------------------|---------------|---------------|---------------|------|
| f <sub>LSICLK</sub>      | Frequency (V <sub>DD</sub> =2-3.6V, T <sub>A</sub> =-40 ~ 105 C)                        | 30            | 45            | 55            | KHz  |
| t <sub>SU</sub> (LSICLK) | Startup time of LSICLK oscillator<br>(V <sub>DD</sub> =3.3V, T <sub>A</sub> =-40~105°C) | -             | 30            | -             | μs   |
| I <sub>DD</sub> (LSICLK) | LSICLK oscillator power consumption                                                     | -             | 0.5           | -             | μA   |

**Note:** According to the comprehensive evaluation, it is not tested in production.

### 5.3.6 Wake-up time in low power mode

**Table 38 Awakening clock source parameters**

| Symbol        | Parameter                 | Typical value | Unit    |
|---------------|---------------------------|---------------|---------|
| $t_{WUSLEEP}$ | Wake up from sleep mode   | 0.52          | $\mu s$ |
| $t_{WUSTOP}$  | Wake up from halt mode    | 24            |         |
| $t_{WUSTDBY}$ | Wake up from standby mode | 80            |         |

**Note:** The wake-up time is measured from the start of the wake-up event to the first instruction read by the user program.

### 5.3.7 PLL characteristics

Table 39 PLL characteristics

| Symbol         | Parameter                                                                             | Numerical value <sup>(1)</sup> |               |               | Unit    |
|----------------|---------------------------------------------------------------------------------------|--------------------------------|---------------|---------------|---------|
|                |                                                                                       | Minimum value                  | Typical value | Maximum value |         |
| $f_{PLL\_IN}$  | PLL input clock                                                                       | 1                              | 8             | 24            | MHz     |
|                | PLL input clock duty cycle                                                            | 40                             | -             | 60            | %       |
| $f_{PLL\_OUT}$ | PLL frequency doubling output clock<br>( $V_{DD}=3.3V$ , $T_A=-40\sim 105^{\circ}C$ ) | 16                             | -             | 48            | MHz     |
| $t_{LOCK}$     | PLL phase locking time                                                                | -                              | -             | 90            | $\mu s$ |

**Note:** According to the comprehensive evaluation, it is not tested in production.

### 5.3.8 Memory characteristics

#### flash memory

Table 40 FLASH memory characteristics

| Symbol      | Parameter                 | Condition                                           | Minimum value | Typical value | Maximum value | Unit    |
|-------------|---------------------------|-----------------------------------------------------|---------------|---------------|---------------|---------|
| $t_{prog}$  | 16-bit programming time   | $T_A=-40\sim 105^{\circ}C$<br>$V_{DD}=2.0\sim 3.6V$ | -             | 3.5           | -             | $\mu s$ |
| $t_{ERASE}$ | Page (1Kbytes) erase time | $T_A=-40\sim 105^{\circ}C$<br>$V_{DD}=2.0\sim 3.6V$ | -             | 39            | -             | ms      |
| $t_{ME}$    | Whole erase time          | $T_A=25^{\circ}C$<br>$V_{DD}=3.3V$                  | -             | 7.2           | -             | ms      |
| $V_{prog}$  | Programming voltage       | $T_A=-40\sim 105^{\circ}C$                          | 2.0           | 3.3           | 3.6           | V       |
| $t_{RET}$   | Data saving time          | $T_A=55^{\circ}C$                                   | 20            | -             | -             | years   |
| $N_{RW}$    | Erase cycle               | $T_A=25^{\circ}C$                                   | 10K           | -             | -             | cycles  |

**Note:** According to the comprehensive evaluation, it is not tested in production.

### 5.3.9 I/O port characteristics

Table 41 Dc characteristics ( $T_A=-40^{\circ}C-105^{\circ}C$ ,  $V_{DD}=2\sim 3.6\text{ v}$ )



| Symbol           | Parameter                            | Condition                                                                   | Minimum value               | Typical value | Maximum value             | Unit |
|------------------|--------------------------------------|-----------------------------------------------------------------------------|-----------------------------|---------------|---------------------------|------|
| V <sub>IL</sub>  | Input low level voltage              | TC and TTa I/O                                                              | -                           | -             | 0.3V <sub>DD</sub> +0.1   | V    |
|                  |                                      | FT and FTf I/O                                                              | -                           | -             | 0.476V <sub>DD</sub> -0.4 |      |
|                  |                                      | I/O pins except BOOT0 pin                                                   | -                           | -             | 0.3V <sub>DD</sub>        |      |
| V <sub>IH</sub>  | Input high level voltage             | TC and TTa I/O                                                              | 0.447V <sub>DD</sub> +0.402 | -             | -                         | V    |
|                  |                                      | FT and FTf I/O                                                              | 0.5V <sub>DD</sub> +0.2     | -             | -                         |      |
|                  |                                      | I/O pins except BOOT0 pin                                                   | 0.7V <sub>DD</sub>          | -             | -                         |      |
| V <sub>hys</sub> | Schmidt trigger hysteresis           | TC and TTa I/O                                                              |                             | 200           |                           | mV   |
|                  |                                      | FT and FTf I/O                                                              |                             | 300           |                           |      |
| I <sub>lk</sub>  | Input leakage current                | V <sub>SS</sub> ≤V <sub>IN</sub> ≤V <sub>DDIOx</sub><br>Standard I / O port | -                           | -             | ±0.1                      | μA   |
|                  |                                      | V <sub>IN</sub> =5V,<br>FT I/O                                              | -                           | -             | 70                        |      |
| R <sub>PU</sub>  | Weak pull-up equivalent resistance   | V <sub>IN</sub> =V <sub>SS</sub>                                            | 30                          | 40            | 50                        | kΩ   |
| R <sub>PD</sub>  | Weak pull-down equivalent resistance | V <sub>IN</sub> =V <sub>DDIOx</sub>                                         | 30                          | 40            | 50                        | kΩ   |

**Table 42 Ac characteristics (T<sub>A</sub> = 25 c)**

| MODEx[1:0]<br>Configuration of | Symbol                  | Parameter                               | Condition                                           | Minimum value | Maximum value | Unit |
|--------------------------------|-------------------------|-----------------------------------------|-----------------------------------------------------|---------------|---------------|------|
| 10 (2MHz)                      | f <sub>max(IO)out</sub> | Maximum frequency                       | C <sub>L</sub> =50 pF,<br>V <sub>DD</sub> =2.4~3.6V | -             | 2             | MHz  |
|                                | t <sub>f(IO)out</sub>   | Output high to low fall time            | C <sub>L</sub> =50 pF,<br>V <sub>DD</sub> =2.4~3.6V | -             | 125           | ns   |
|                                | t <sub>r (IO)out</sub>  | Output rise time from low to high level |                                                     | -             | 125           |      |
| 01 (10MHz)                     | f <sub>max(IO)out</sub> | Maximum frequency                       | C <sub>L</sub> =50 pF,<br>V <sub>DD</sub> =2.4~3.6V | -             | 10            | MHz  |
|                                | t <sub>f(IO)out</sub>   | Output high to low fall time            | C <sub>L</sub> =50 pF,<br>V <sub>DD</sub> =2.4~3.6V | -             | 25            | ns   |
|                                | t <sub>r (IO)out</sub>  | Output rise time from low to high level |                                                     | -             | 25            |      |

| MODEx[1:0]<br>Configuration<br>of | Symbol                          | Parameter                                     | Condition                                                    | Minimum<br>value | Maximum<br>value | Unit |
|-----------------------------------|---------------------------------|-----------------------------------------------|--------------------------------------------------------------|------------------|------------------|------|
| 11 (50MHz)                        | $f_{\max(\text{IO})\text{out}}$ | Maximum<br>frequency                          | $C_L=30\text{ pF}$ ,<br>$V_{DD}=2.7\sim 3.6\text{V}$         | -                | 50               | MHz  |
|                                   | $t_{f(\text{IO})\text{out}}$    | Output high to low<br>fall time               | $C_L=30\text{ pF}$ ,<br>$V_{DD}=2.7\sim 3.6\text{V}$         | -                | 5                | ns   |
|                                   | $t_{r(\text{IO})\text{out}}$    | Output rise time<br>from low to high<br>level |                                                              | -                | 5                |      |
| FM+<br>configuration              | $f_{\max(\text{IO})\text{out}}$ | Maximum<br>frequency <sup>(3)</sup>           | $C_L=50\text{pF}$ ,<br>$V_{DDIOx}$<br>$=2.4\sim 3.6\text{V}$ | -                | 2                | MHz  |
|                                   | $t_{f(\text{IO})\text{out}}$    | Output falling time                           |                                                              | -                | 34               | ns   |
|                                   | $t_{r(\text{IO})\text{out}}$    | Output rise time                              |                                                              | -                | 34               |      |

Figure 14 Definition of input and output AC characteristics

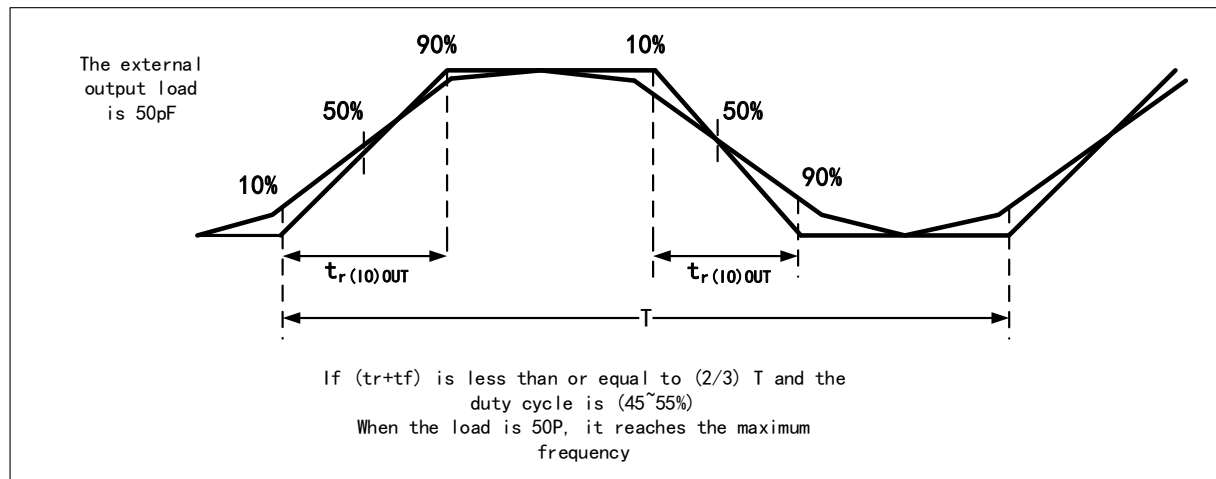


Table 43 Output drive current characteristics ( $T_A=25^\circ\text{C}$ )

| Symbol   | Parameter                    | Condition                                              | Min             | Max | Unit |
|----------|------------------------------|--------------------------------------------------------|-----------------|-----|------|
| $V_{OL}$ | I/O pin outputs low voltage  | $ I_{IO} =8\text{ mA}$<br>$V_{DDIOx}\geq 2.7\text{V}$  | -               | 0.4 | V    |
| $V_{OH}$ | I/O pin outputs high voltage |                                                        | $V_{DDIOx}-0.4$ | -   |      |
| $V_{OL}$ | I/O pin outputs low voltage  | $ I_{IO} =20\text{ mA}$<br>$V_{DDIOx}\geq 2.7\text{V}$ | -               | 1.3 | V    |
| $V_{OH}$ | I/O pin outputs high voltage |                                                        | $V_{DDIOx}-1.3$ | -   |      |

### 5.3.10 NRST pin characteristics

The NRST pin input drive adopts CMOS process, which is connected with a permanent pull-up resistor  $R_{PU}$ .

Table 44 NRST pin characteristics ( $T_A = -40 \sim 105^\circ\text{C}$ ,  $V_{CC} = 2 \sim 3.6\text{ V}$ )

| Symbol                | Parameter              | Condition | Min | Typ | Max                | Unit |
|-----------------------|------------------------|-----------|-----|-----|--------------------|------|
| $V_{IL(\text{NRST})}$ | NRST input low voltage | -         | -   | -   | $0.31V_{DD}+0.065$ | V    |

| Symbol          | Parameter                                  | Condition       | Min                 | Typ | Max | Unit       |
|-----------------|--------------------------------------------|-----------------|---------------------|-----|-----|------------|
| $V_{IH(NRST)}$  | NRST input high voltage                    | -               | $0.446V_{DD}+0.405$ |     |     |            |
| $V_{hys(NRST)}$ | Voltage hysteresis of NRST Schmitt trigger | -               | -                   | 300 | -   | mV         |
| $R_{PU}$        | Weak pull-up equivalent resistance         | $V_{IN}=V_{SS}$ | 30                  | 40  | 50  | k $\Omega$ |

### 5.3.11 communication interface

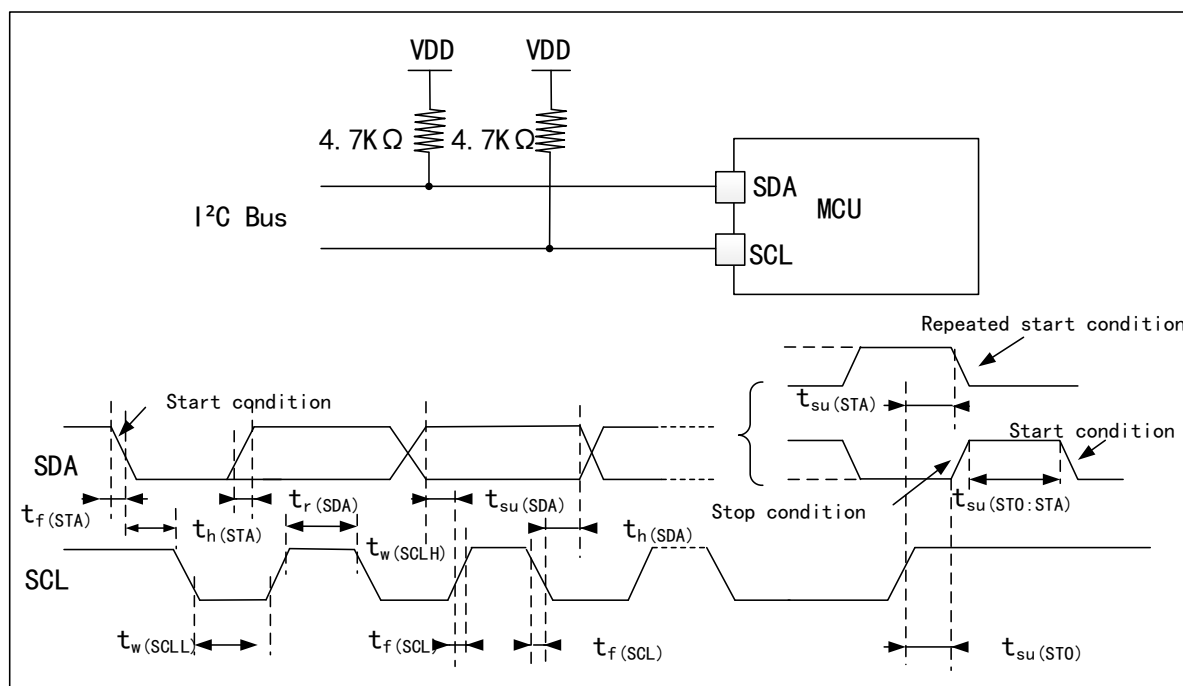
#### I2C interface characteristics

- Standard mode (Sm): bit rate up to 100kbit/s
- Fast mode (Fm): bit rate up to 400 kbit/s
- Ultra fast mode (Fm+): bit rate up to 1Mbit/s

Table 45 I2C interface characteristics ( $T_A = 25^{\circ}\text{C}$ ,  $V_{DD} = 3.3\text{ V}$ )

| Symbol                   | Parameter                                              | Standard I2C |      | Fast I2C |      | Ultrafast I2C |     | Unit          |
|--------------------------|--------------------------------------------------------|--------------|------|----------|------|---------------|-----|---------------|
|                          |                                                        | Min          | Max  | Min      | Max  | Min           | Max |               |
| $t_{w(SCLL)}$            | SCL clock low time                                     | 4.84         | -    | 1.21     | -    | 0.52          | -   | $\mu\text{s}$ |
| $t_{w(SCLH)}$            | SCL clock high time                                    | 5.09         | -    | 1.14     | -    | 0.46          | -   |               |
| $t_{su(SDA)}$            | SDA setup time                                         | 4460         | -    | 860      | -    | 321           | -   | ns            |
| $t_h(SDA)$               | SDA data holding time                                  | 103          | 181  | 0        | 252  | 0             | 145 |               |
| $t_r(SDA)$<br>$t_r(SCL)$ | SDA and SCL rise time                                  | -            | 500  | -        | 300  | -             | 120 |               |
| $t_f(SDA)$<br>$t_f(SCL)$ | SDA and SCL fall time                                  | -            | 9.86 | -        | 8.12 | -             | 4   |               |
| $t_h(STA)$               | Start condition holding time                           | 4.96         | -    | 1        |      | 0.33          | -   | $\mu\text{s}$ |
| $t_{su(STA)}$            | Repeated start condition setup time                    | 5.16         | -    | 1.21     | -    | 0.64          | -   |               |
| $t_{su(STO)}$            | Setup time of stop condition                           | 4.50         | -    | 1.21     | -    | 0.54          | -   | $\mu\text{s}$ |
| $t_{w(STO:STA)}$         | Time from stop condition to start condition (bus idle) | 4.67         | -    | 1.37     | -    | 0.77          | -   | $\mu\text{s}$ |

Figure 15 Bus AC waveform and measurement circuit



**Note:** The measuring points are set at CMOS levels:  $0.3V_{DD}$  and  $0.7V_{DD}$ .

### SPI interface characteristics

Table 46 SPI characteristics ( $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.3\text{ V}$ )

| Symbol                       | Parameter                    | Condition                                                           | Min | Max | Unit |
|------------------------------|------------------------------|---------------------------------------------------------------------|-----|-----|------|
| $f_{SCK}$<br>$1/t_c(SCK)$    | SPI clock frequency          | holotype                                                            | -   | 18  | MHz  |
|                              |                              | Slave mode                                                          | -   | 18  |      |
| $t_r(SCK)$<br>$t_f(SCK)$     | SPI clock rise and fall time | Load capacitance: $C = 15\text{pF}$                                 | -   | 6   | ns   |
| $t_{su}(NSS)$                | NSS setup time               | Slave mode                                                          | 223 | -   | ns   |
| $t_h(NSS)$                   | NSS holding time             | Slave mode                                                          | 65  | -   | ns   |
| $t_w(SCKH)$<br>$t_w(SCKL)$   | SCK high and low time        | Main mode, $f_{PCMU} = 36\text{MHz}$ ,<br>Prescaler coefficient = 4 | 54  | 57  | ns   |
| $t_{su}(MI)$<br>$t_{su}(SI)$ | Data input setup time        | holotype                                                            | 12  | -   | ns   |
|                              |                              | Slave mode                                                          | 20  | -   |      |
| $t_h(MI)$<br>$t_h(SI)$       | Data input holding time      | holotype                                                            | 34  | -   | ns   |
|                              |                              | Slave mode                                                          | 22  | -   |      |
| $t_a(SO)$                    | Data output access time      | In slave mode, $f_{PCLK} = 20\text{MHz}$                            | -   | 17  | ns   |
| $t_{dis}(SO)$                | Data output prohibition time | Slave mode                                                          | -   | 18  | ns   |

| Symbol      | Parameter                     | Condition                       | Min  | Max | Unit |
|-------------|-------------------------------|---------------------------------|------|-----|------|
| $t_{v(SO)}$ | Effective time of data output | Slave mode (after enable edge)  | -    | 16  | ns   |
| $t_{v(MO)}$ | Effective time of data output | Master mode (after enable edge) | -    | 6   | ns   |
| $t_{h(SO)}$ | Data output holding time      | Slave mode (after enable edge)  | 11.5 | -   | ns   |
| $t_{h(MO)}$ |                               | Master mode (after enable edge) | 2    | -   |      |

Figure 16 SPI timing diagram—slave mode and CPHA=0

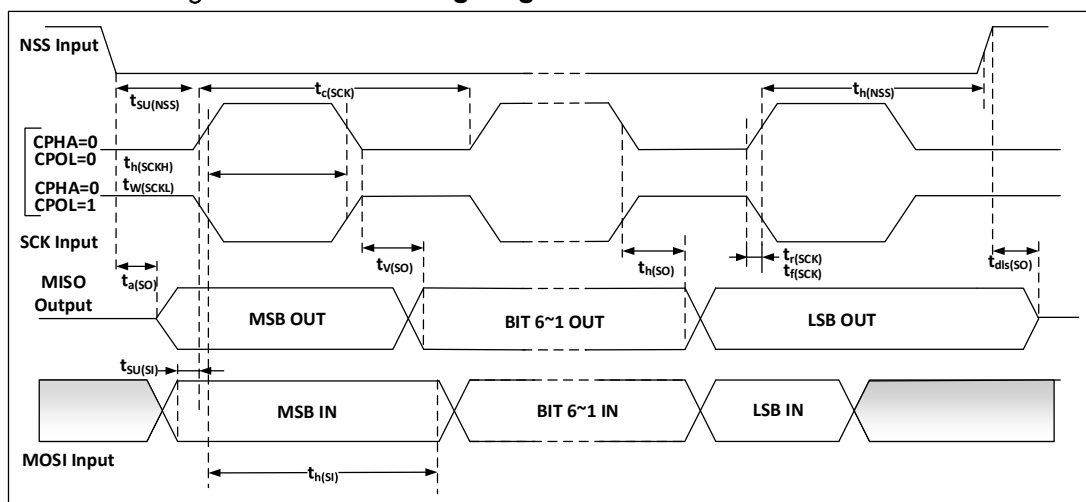
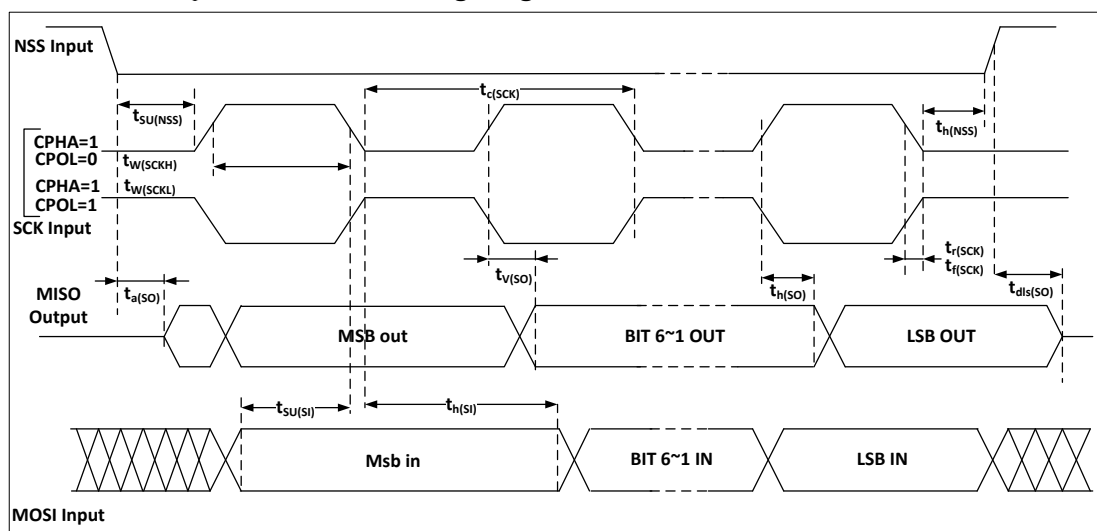
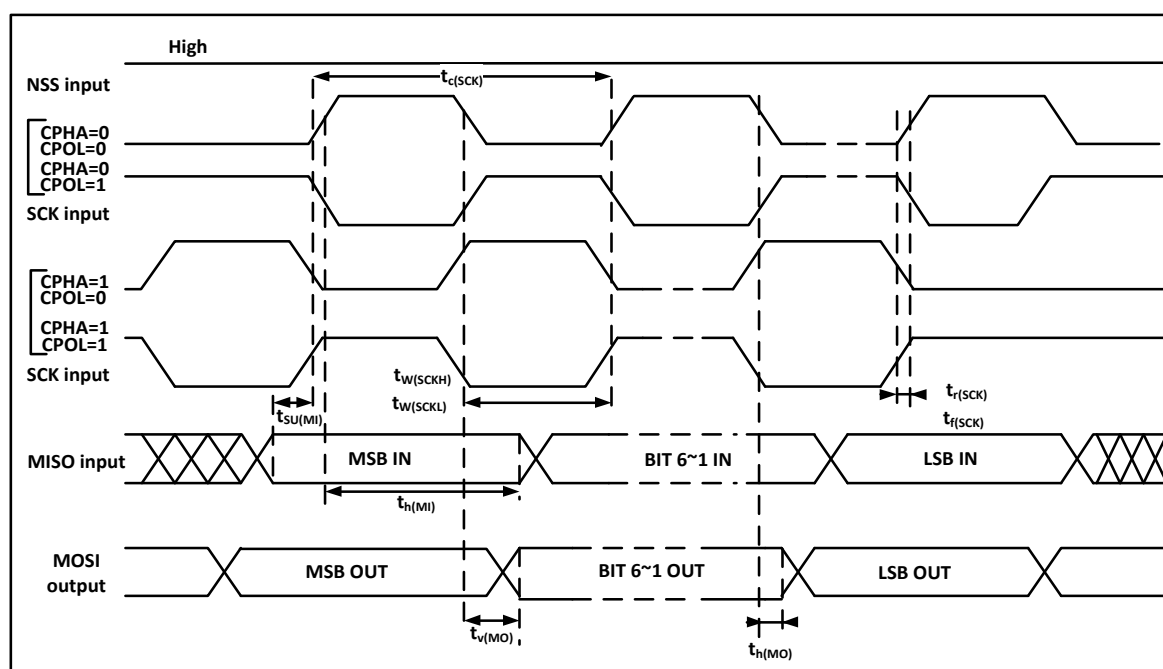


Figure 17 SPI timing diagram—slave mode and CPHA=1



Note: The measuring points are set at CMOS levels: 0.3V<sub>DD</sub> and 0.7V<sub>DD</sub>.

Figure 18 SPI timing diagram—main mode



Note: The measuring points are set at CMOS levels:  $0.3V_{DD}$  and  $0.7V_{DD}$ .

### 5.3.12 12-bit ADC features

Table 47 12-bit ADC features

| Symbol     | Parameter                                 | Condition                                         | Minimum value | Typical value | Maximum value | Unit     |
|------------|-------------------------------------------|---------------------------------------------------|---------------|---------------|---------------|----------|
| $V_{DDA}$  | Service voltage                           | -                                                 | 2.4           | -             | 3.6           | V        |
| $f_{ADC}$  | ADC frequency                             | -                                                 | 0.6           | -             | 14            | MHz      |
| $C_{ADC}$  | Internal sampling and holding capacitance | -                                                 | -             | 8             | -             | pF       |
| $R_{ADC}$  | Sampling resistance                       | -                                                 | -             | -             | 1000          | $\Omega$ |
| $t_s$      | Sampling time                             | $f_{ADC} = 14 \text{ MHz}$                        | 0.107         | -             | 17.1          | $\mu s$  |
| $T_{CONV}$ | Sampling and conversion Time              | $f_{ADC} = 14 \text{ MHz}$ ,<br>12-bit conversion | 1             | -             | 18            | $\mu s$  |

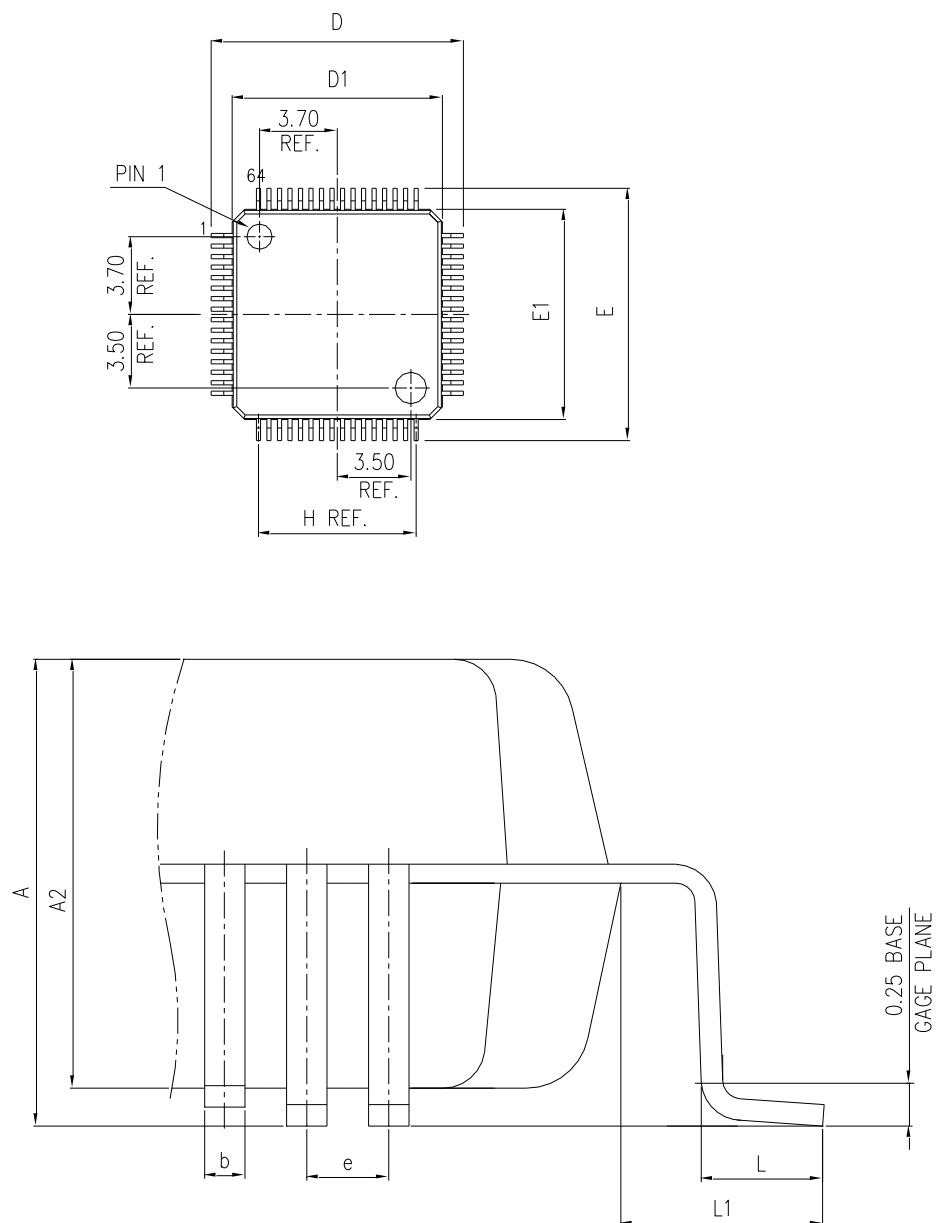
Table 48 12-bit ADC accuracy

| Symbol  | Parameter                 | Condition                                                                                         | Typical value | Maximum value | Unit |
|---------|---------------------------|---------------------------------------------------------------------------------------------------|---------------|---------------|------|
| $ E_T $ | Composite error           | $f_{PCLK}=48M$ ,<br>$f_{ADC}=14M$ ,<br>$V_{DDA}=2.4V-3.6V$<br>$T_A=-40^{\circ}C\sim 105^{\circ}C$ | 2.18          | 4.0           | LSB  |
| $ E_O $ | offset error              |                                                                                                   | 0.7           | 3             |      |
| $ E_G $ | Gain error                |                                                                                                   | 0.32          | 1.3           |      |
| $ E_D $ | Differential linear error |                                                                                                   | 1.0           | 1.3           |      |
| $ E_L $ | Integral linearity error  |                                                                                                   | 1.62          | 2.3           |      |

## 6. Package Characteristics

### 6.1. LQFP64 package information

Figure 19 LQFP64 package outline



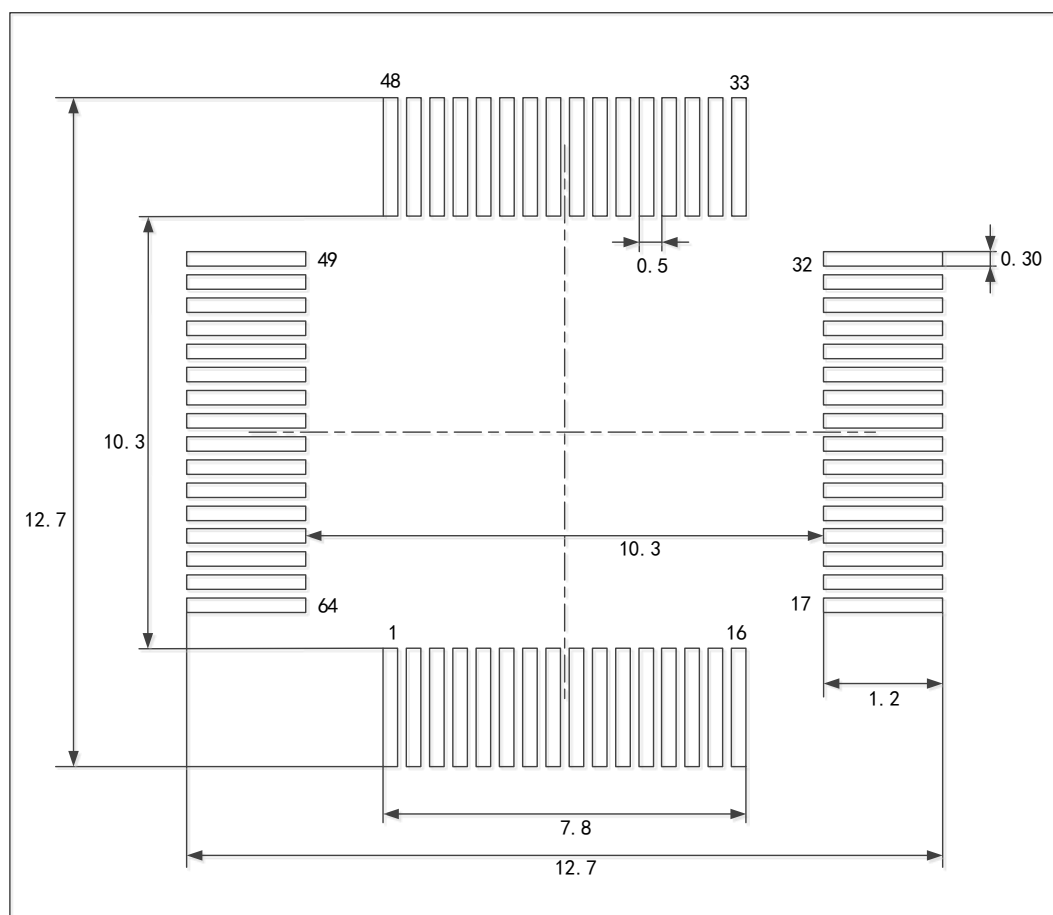
**Note:** The Figure is not drawn to scale.

Table 49 Package dimensions of LQFP64

| S/N | SYM     | DIMENSIONS   | REMARKS         |
|-----|---------|--------------|-----------------|
| 1   | A       | MAX.1.600    | OVERALL HEIGHT  |
| 2   | A2      | 1.400±0.050  | PKG THICKNESS   |
| 3   | D       | 12.000±0.200 | LEAD TIP TO TIP |
| 4   | D1      | 10.000±0.100 | PKG LENGTH      |
| 5   | E       | 12.000±0.200 | LEAD TIP TO TIP |
| 6   | E1      | 10.000±0.100 | PKG WIDTH       |
| 7   | L       | 0.600±0.150  | FOOT LENGTH     |
| 8   | L1      | 1.000 REF.   | LEAD LENGTH     |
| 9   | e       | 0.500 BASE   | LEAD PITCH      |
| 10  | H(REF.) | (7.500)      | GUM.LEAD PITCH  |
| 11  | b       | 0.220±0.050  | LEAD WIDTH      |

**Note:** The value in inches is converted from mm to 4 decimal places.

Figure 20 LQFP64 welding Layout suggestion



**Note:** Dimensions are in millimeters.

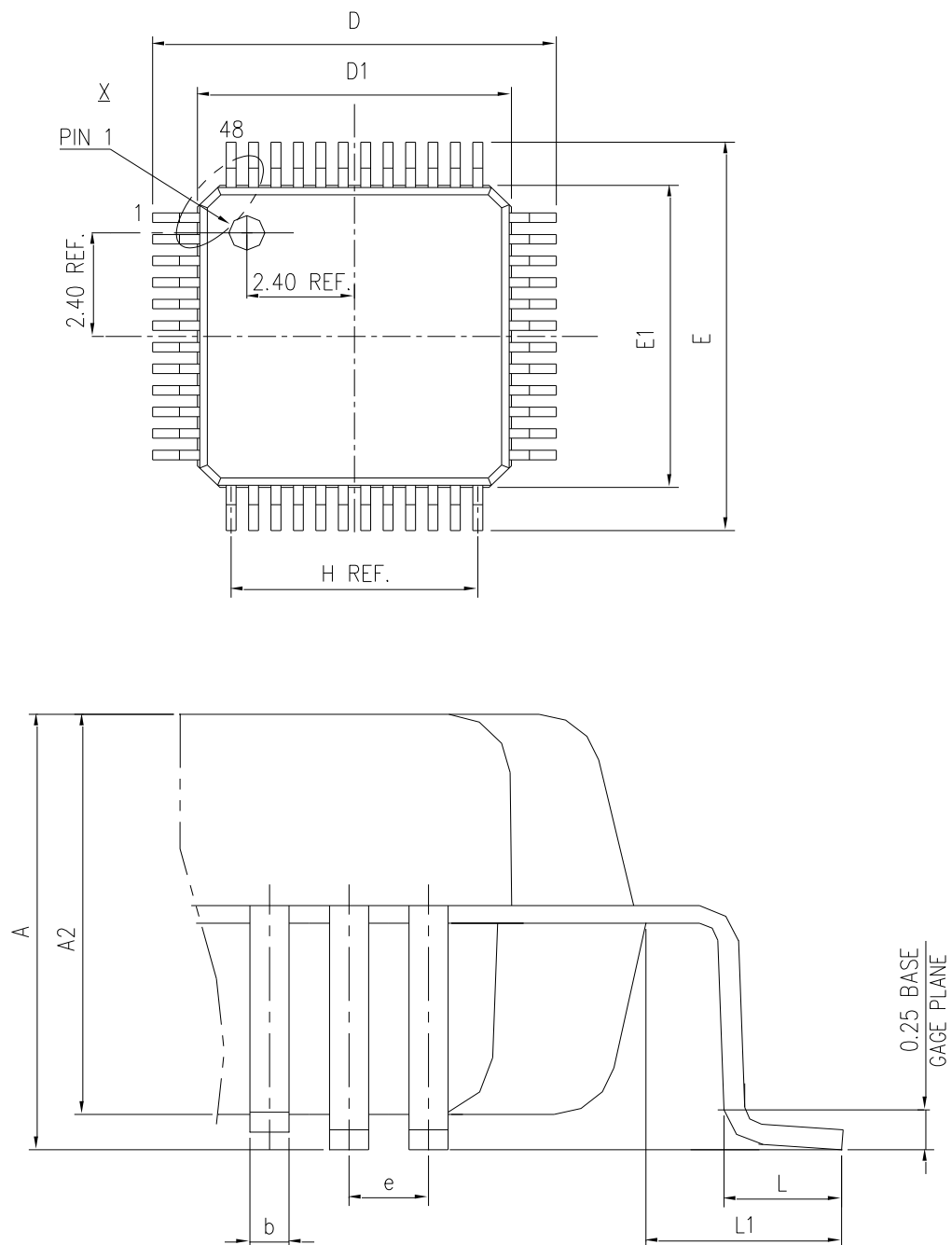


Figure 21 LQFP64 coding specification



## 6.2. LQFP48 package information

Figure 22 LQFP48 package outline



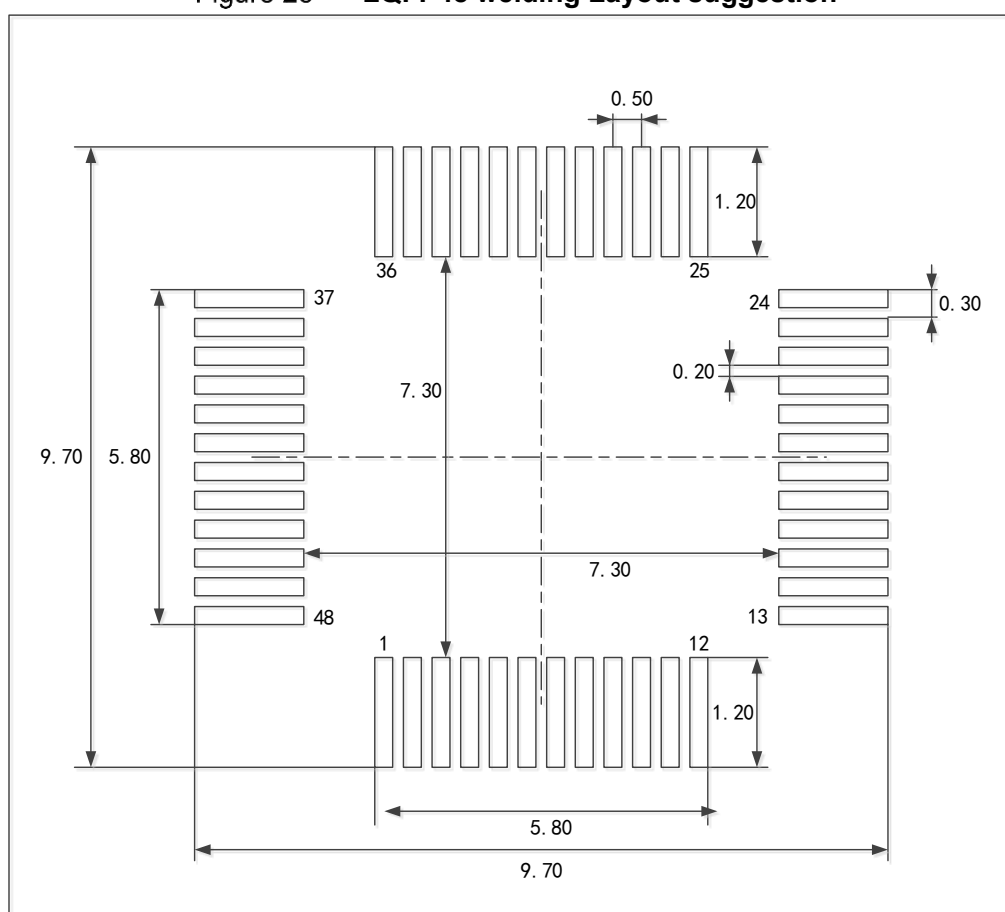
**Note:** The Figure is not drawn to scale.

Table 50 Package dimensions of LQFP48

| S/N | SYM     | DIMENSIONS | REMARKS         |
|-----|---------|------------|-----------------|
| 1   | A       | MAX.1.60   | OVERALL HEIGHT  |
| 2   | A2      | 1.40±0.05  | PKG THICKNESS   |
| 3   | D       | 9.00±0.20  | LEAD TIP TO TIP |
| 4   | D1      | 7.00±0.10  | PKG LENGTH      |
| 5   | E       | 9.00±0.20  | LEAD TIP TO TIP |
| 6   | E1      | 7.00±0.10  | PKG WIDTH       |
| 7   | L       | 0.60±0.15  | FOOT LENGTH     |
| 8   | L1      | 1.00 REF.  | LEAD LENGTH     |
| 9   | e       | 0.50 BASE  | LEAD PITCH      |
| 10  | H(REF.) | ( 5.50 )   | GUM.LEAD PITCH  |
| 11  | b       | 0.22±0.050 | LEAD WIDTH      |

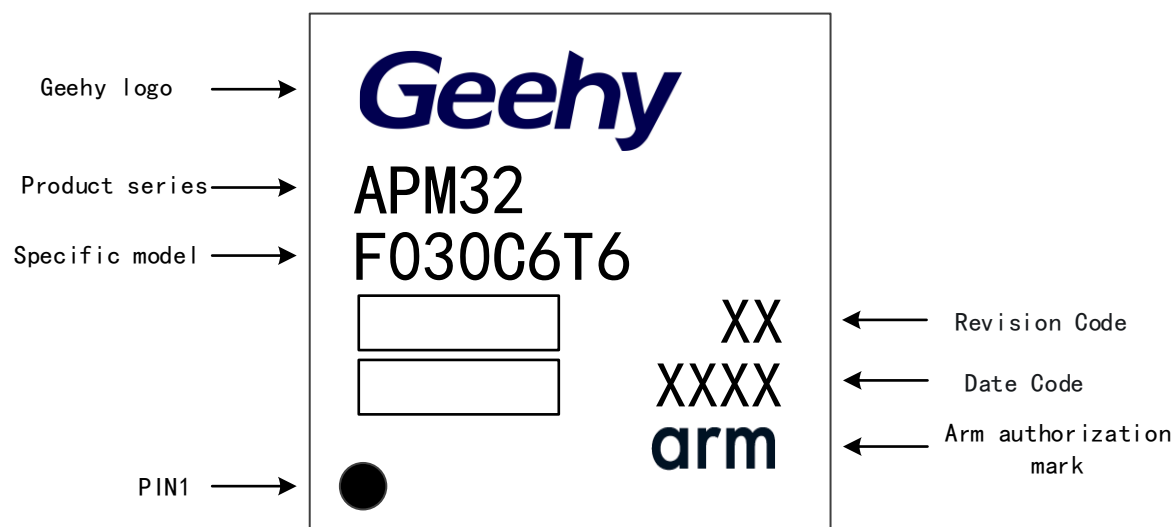
**Note:** The value in inches is converted from mm to 4 decimal places.

Figure 23 LQFP48 welding Layout suggestion



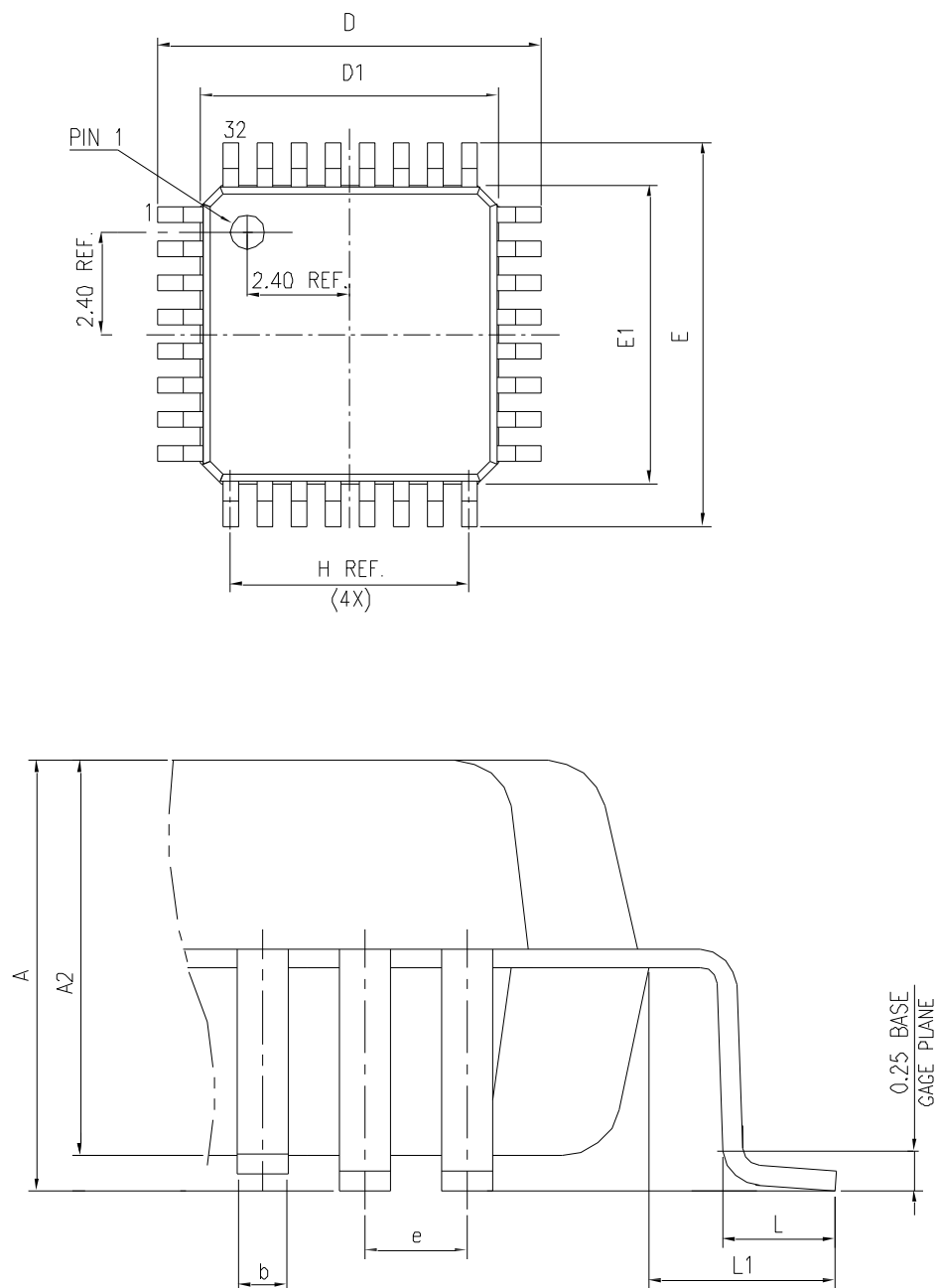
**Note:** Dimensions are in millimeters.

Figure 24 LQFP48 coding specification



### 6.3. LQFP32 package information

Figure 25 LQFP32 package outline



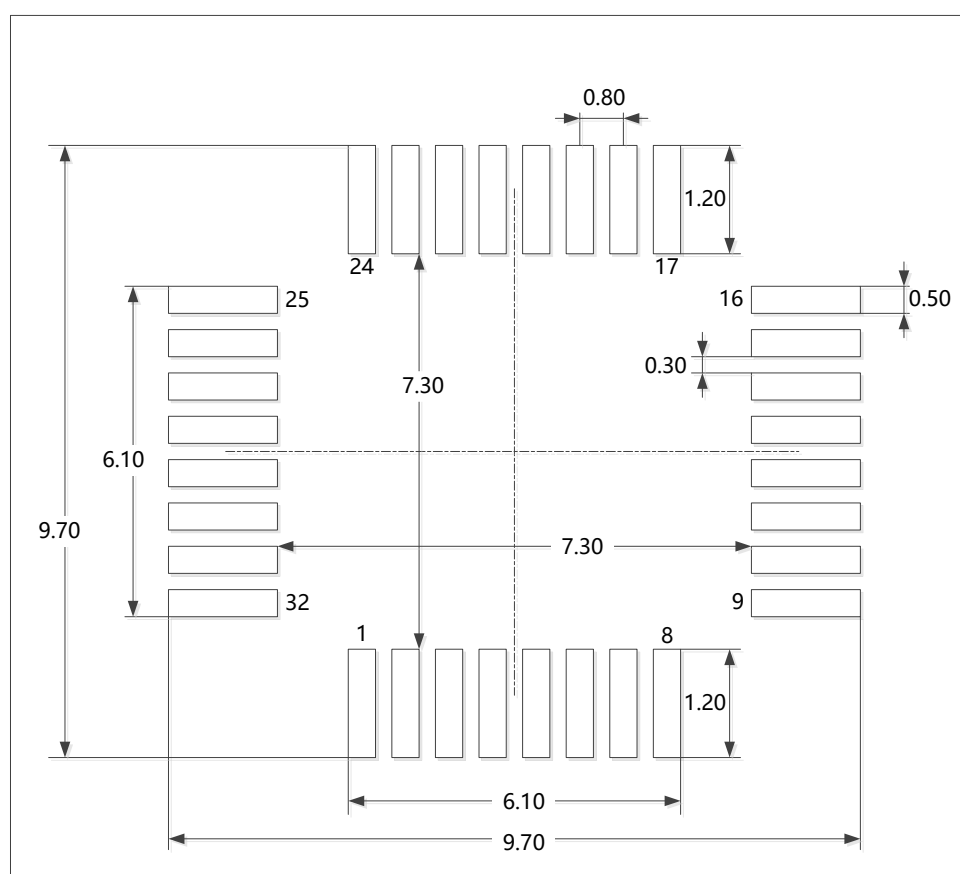
**Note:** The Figure is not drawn to scale.

Table 51 Package dimensions of LQFP32

| S/N | SYM     | DIMENSIONS        | REMARKS         |
|-----|---------|-------------------|-----------------|
| 1   | A       | MAX.1.6           | OVERALL HEIGHT  |
| 2   | A2      | 1.40±0.05         | PKG THICKNESS   |
| 3   | D       | 9.00±0.20         | LEAD TIP TO TIP |
| 4   | D1      | 7.00±0.10         | PKG LENGTH      |
| 5   | E       | 9.00±0.20         | LEAD TIP TO TIP |
| 6   | E1      | 7.00±0.10         | PKG WIDTH       |
| 7   | L       | 0.60±0.15         | FOOT LENGTH     |
| 8   | L1      | 1.00 REF.         | LEAD LENGTH     |
| 9   | e       | 0.80 BASE         | LEAD PITCH      |
| 10  | H(REF.) | ( 5.60 )          | GUM.LEAD PITCH  |
| 11  | b       | 0.370±0.080/0.070 | LEAD WIDTH      |

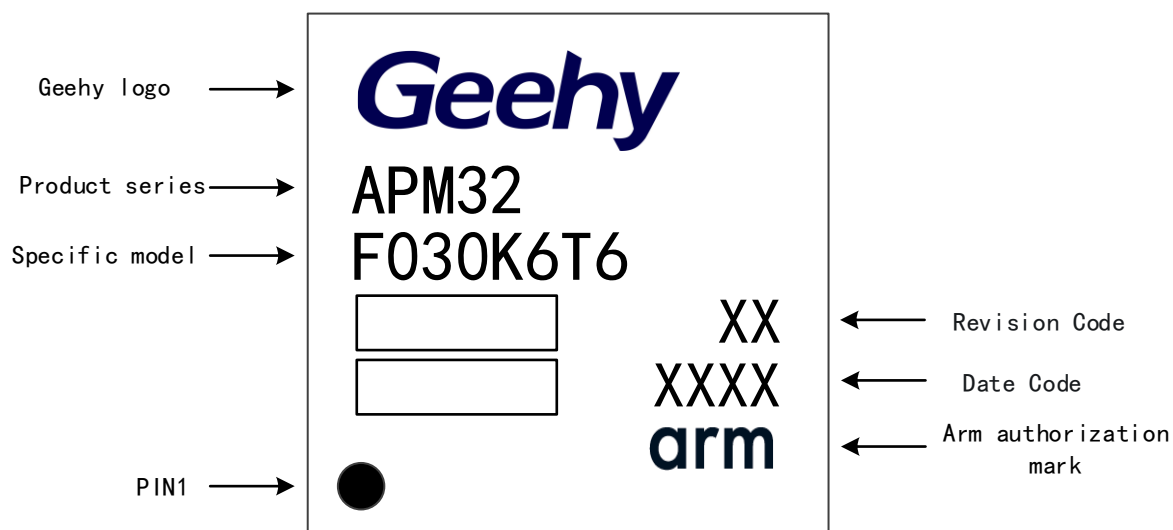
**Note:** The value in inches is converted from mm to 4 decimal places.

Figure 26 LQFP32 welding Layout suggestion



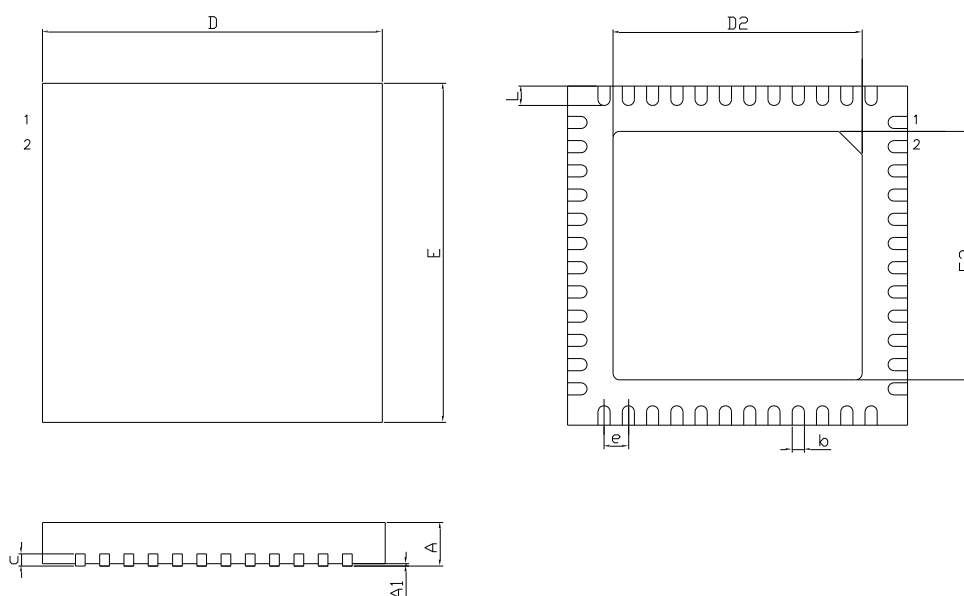
**Note:** Dimensions are in millimeters.

Figure 27 LQFP32 coding specification



## 6.4. QFN48 package information

Figure 28 QFN48 package outline



Note: The Figure is not drawn to scale.

Table 52 Package dimensions of QFN48

| SYMBOL | MILLIMETER |      |      |
|--------|------------|------|------|
|        | MIN        | NOM  | MAX  |
| A      | 0.7        | 0.75 | 0.8  |
| A1     | -          | 0.02 | 0.05 |

Figure 29 QFN48 welding Layout suggestion

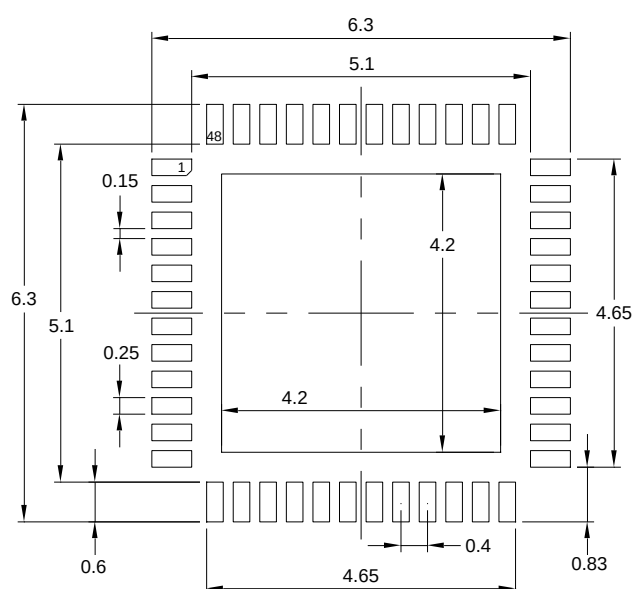
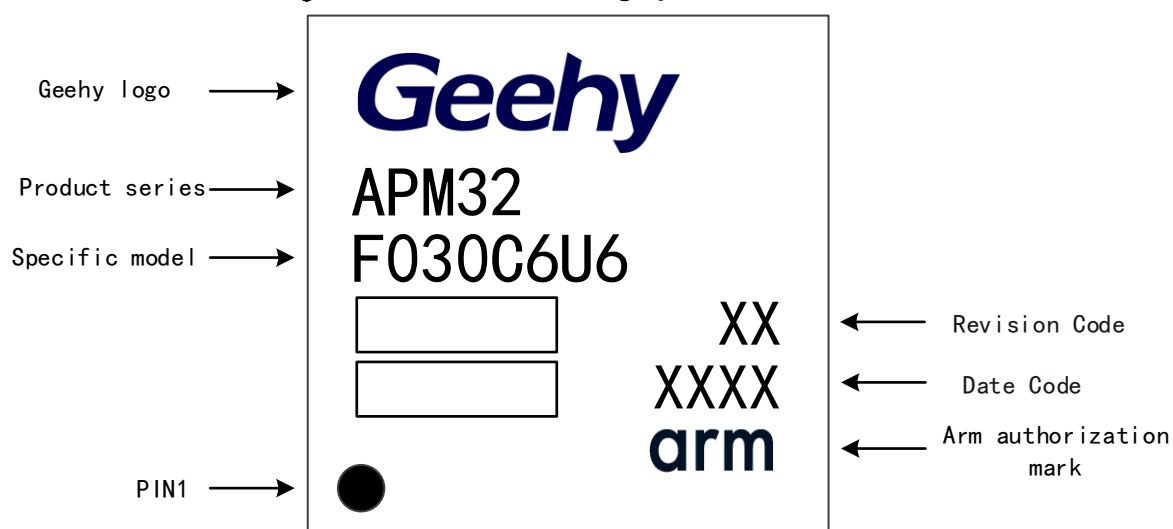




Figure 30 QFN48 coding specification



## 6.5. QFN32 Package information

Figure 31 QFN32 package outline

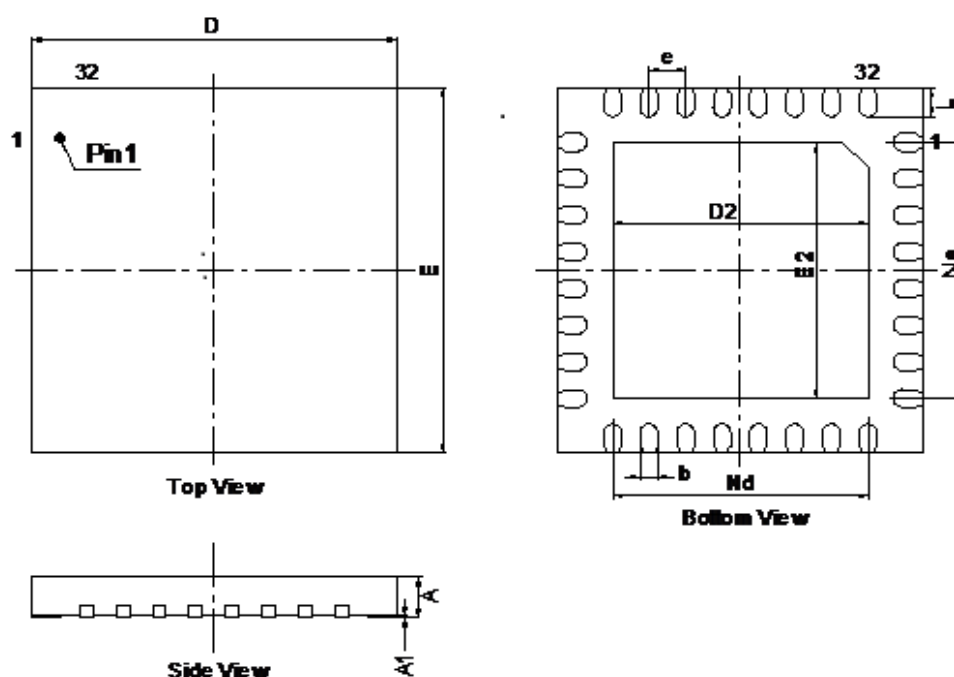


Table 53 QFN32 Package dimensions

| SYMBOL | MILLIMETER |      |     |
|--------|------------|------|-----|
|        | MIN        | NOM  | MAX |
| A      | 0.5        | 0.55 | 0.6 |

| SYMBOL | MILLIMETER |      |      |
|--------|------------|------|------|
| A1     | 0          | 0.02 | 0.05 |
| b      | 0.19       | 0.24 | 0.29 |
| D      | 4.9        | 5    | 5.1  |
| D2     | 3.4        | 3.5  | 3.6  |
| e      | 0.50BSC    |      |      |
| Nd     | 3.50BSC    |      |      |
| E      | 4.9        | 5    | 5.1  |
| E2     | 3.4        | 3.5  | 3.6  |
| Ne     | 3.50BSC    |      |      |
| L      | 0.35       | 0.4  | 0.45 |

Figure 32 QFN32 welding Layout suggestion

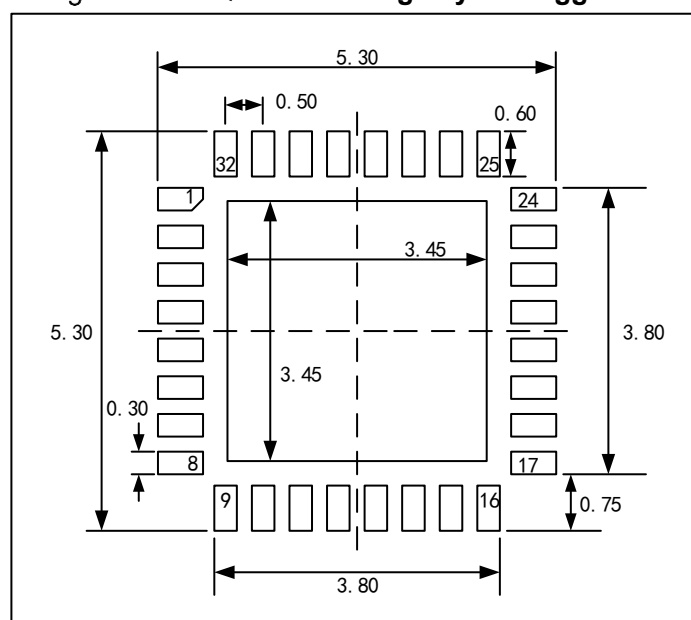
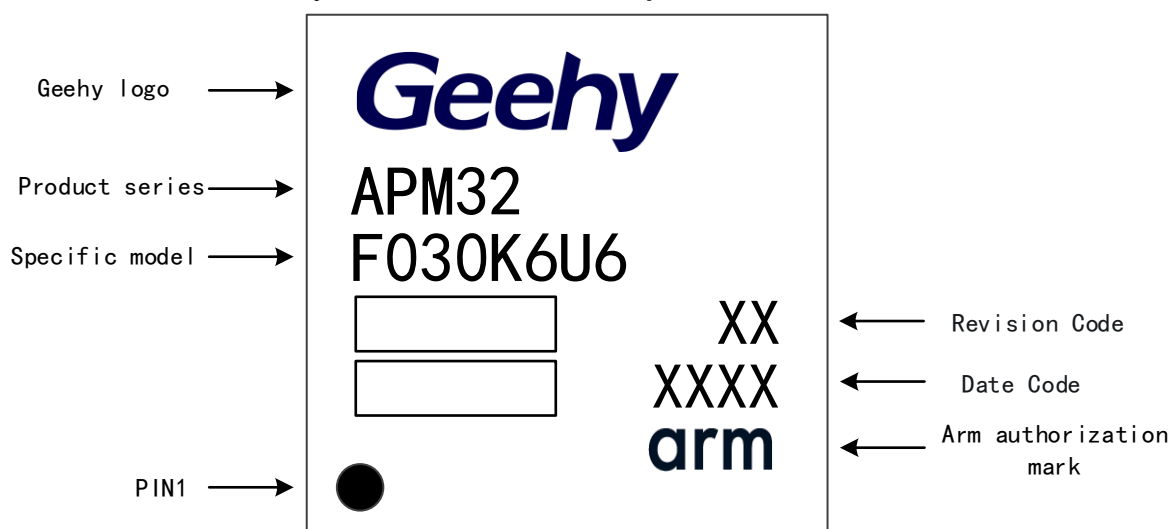
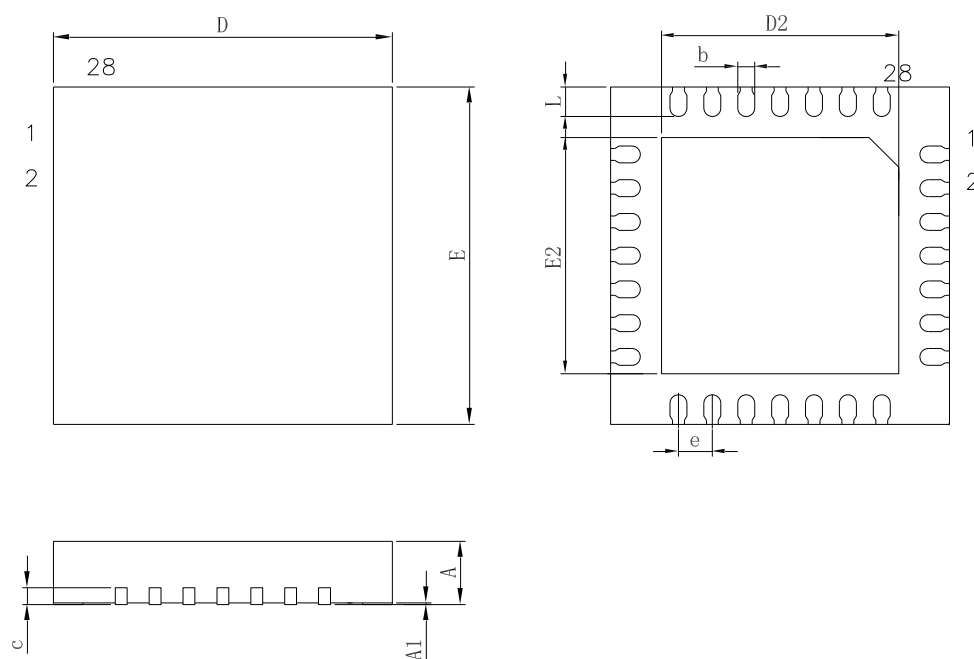


Figure 33 QFN32 Code specification



## 6.6. QFN28 Package information

Figure 34 QFN28 package outline



**Note:** The Figure is not drawn to scale.

Table 54 QFN28 Package dimensions

| SYMBOL | MILLIMETER |      |      |
|--------|------------|------|------|
|        | MIN        | NOM  | MAX  |
| A      | 0.70       | 0.75 | 0.80 |
| A1     | 0          | 0.02 | 0.05 |
| b      | 0.15       | 0.20 | 0.25 |
| c      | 0.18       | 0.20 | 0.25 |
| D      | 3.90       | 4.00 | 4.10 |
| D2     | 2.70       | 2.80 | 2.90 |
| e      | 0.40BSC    |      |      |
| E      | 3.90       | 4.00 | 4.10 |
| E2     | 2.70       | 2.80 | 2.90 |
| L      | 0.30       | 0.35 | 0.40 |

**Note:** The value in inches is converted from mm to 4 decimal places.

Figure 35 QFN28 welding Layout suggestion

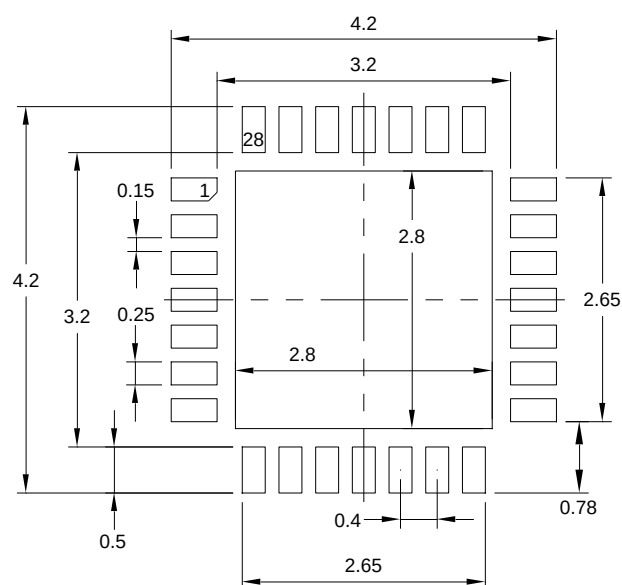
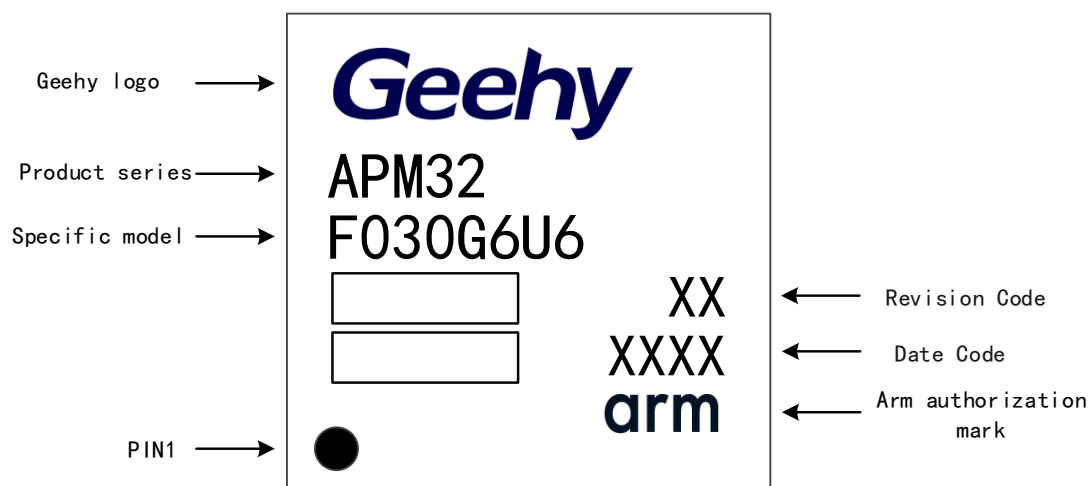


Figure 36 QFN28 Code specification



## 6.7. TSSOP20 Package information

Figure 37 TSSOP20 Package information

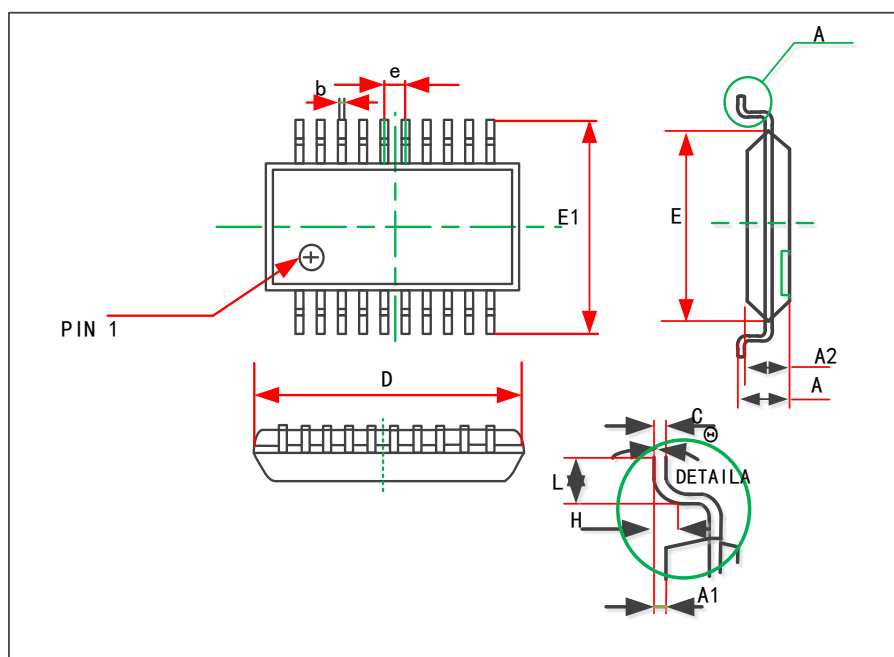
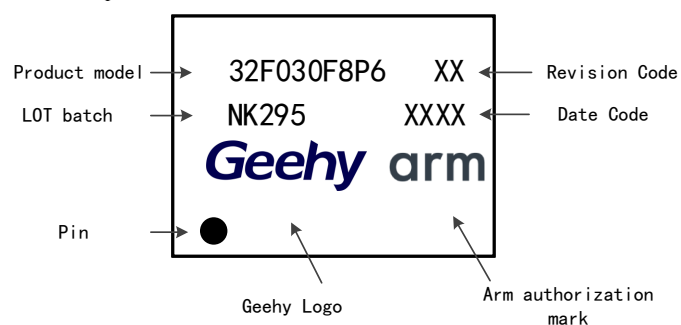


Table 55 TSSOP20 Package dimensions

| SYMBOL | Dimensions IN Millimeters |       | Dimensions IN Inches |       |
|--------|---------------------------|-------|----------------------|-------|
|        | MIN                       | MAX   | MIN                  | MAX   |
| D      | 6.400                     | 6.600 | 0.252                | 0.259 |
| E      | 4.300                     | 4.500 | 0.169                | 0.177 |
| b      | 0.190                     | 0.300 | 0.007                | 0.012 |
| c      | 0.090                     | 0.200 | 0.004                | 0.008 |
| E1     | 6.250                     | 6.550 | 0.246                | 0.258 |
| A      | -                         | 1.200 | -                    | 0.047 |
| A2     | 0.800                     | 1.000 | 0.031                | 0.039 |
| A1     | 0.050                     | 0.150 | 0.002                | 0.006 |
| e      | 0.65(BSC)                 |       | 0.026(BSC)           |       |
| L      | 0.500                     | 0.700 | 0.020                | 0.028 |
| H      | 0.25(TYP)                 |       | 0.01(TYP)            |       |
| θ      | 1°                        | 7°    | 1°                   | 7°    |

Figure 38 TSSOP20 Code specification



## 7. Ordering information

|                              | APM32                                                                                                  | F | 030 | R | 8 | T | X | XXX |
|------------------------------|--------------------------------------------------------------------------------------------------------|---|-----|---|---|---|---|-----|
| <b>Product series</b>        | APM32=ARM-based 32-bit MCU                                                                             |   |     |   |   |   |   |     |
| <b>Product type</b>          | F=General type                                                                                         |   |     |   |   |   |   |     |
| <b>Product subseries</b>     | 030=Basic type                                                                                         |   |     |   |   |   |   |     |
| <b>Number of pins</b>        | F=20 pins<br>G=28 pins<br>K=32 pins<br>C=48 pins<br>R=64 pins                                          |   |     |   |   |   |   |     |
| <b>Flash memory capacity</b> | 4 =16 Kbytes<br>6 =32 Kbytes<br>8 =64 Kbytes                                                           |   |     |   |   |   |   |     |
| <b>Package</b>               | P=TSSOP<br>T=LQFP<br>U=QFN                                                                             |   |     |   |   |   |   |     |
| <b>Temperature range</b>     | 6=Industrial-grade temperature range; -40°C~85°C<br>7= Industrial-grade temperature range; -40°C~105°C |   |     |   |   |   |   |     |
| <b>Option</b>                | XXX=Programmed device code<br>R=Reel package<br>Blank=Tray package<br>T=Tube package                   |   |     |   |   |   |   |     |

**Table 56 Order information list**

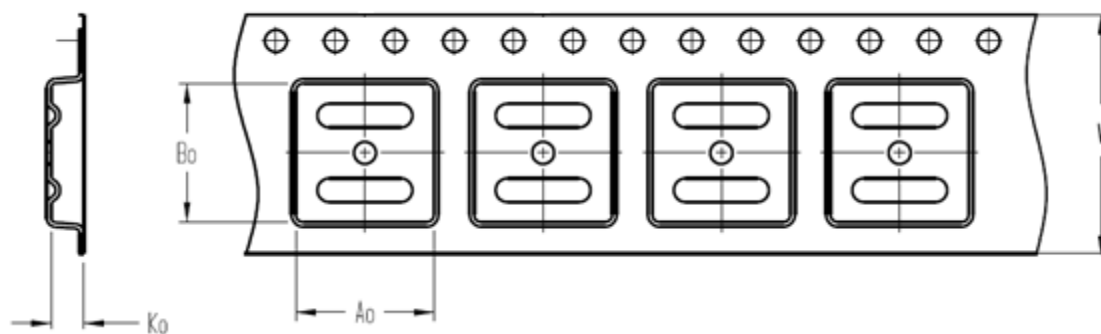
| Order code      | FLASH(KB) | SRAM(KB) | Package | SPQ   | Temperature range           |
|-----------------|-----------|----------|---------|-------|-----------------------------|
| APM32F030F4P6-T | 16        | 8        | TSSOP20 | 14720 | Industrial grade -40°C~85°C |
| APM32F030F6P6-T | 32        | 8        | TSSOP20 | 14720 | Industrial grade -40°C~85°C |
| APM32F030F8P6-T | 64        | 8        | TSSOP20 | 14720 | Industrial grade -40°C~85°C |
| APM32F030F4P6-R | 16        | 8        | TSSOP20 | 4000  | Industrial grade -40°C~85°C |
| APM32F030F6P6-R | 32        | 8        | TSSOP20 | 4000  | Industrial grade -40°C~85°C |
| APM32F030F8P6-R | 64        | 8        | TSSOP20 | 4000  | Industrial grade -40°C~85°C |
| APM32F030G4U6   | 16        | 8        | QFN28   | 4900  | Industrial grade -40°C~85°C |
| APM32F030G6U6   | 32        | 8        | QFN28   | 4900  | Industrial grade -40°C~85°C |
| APM32F030G8U6   | 64        | 8        | QFN28   | 4900  | Industrial grade -40°C~85°C |
| APM32F030K6U6-R | 32        | 4        | QFN32   | 5000  | Industrial grade -40°C~85°C |
| APM32F030K6U6   | 32        | 4        | QFN32   | 4900  | Industrial grade -40°C~85°C |
| APM32F030C6U6   | 32        | 8        | QFN48   | 4900  | Industrial grade -40°C~85°C |
| APM32F030C8U6   | 64        | 8        | QFN48   | 4900  | Industrial grade -40°C~85°C |
| APM32F030K6T6-R | 32        | 4        | LQFP32  | 2000  | Industrial grade -40°C~85°C |
| APM32F030K6T6   | 32        | 4        | LQFP32  | 2500  | Industrial grade -40°C~85°C |
| APM32F030K8T6-R | 64        | 8        | LQFP32  | 2000  | Industrial grade -40°C~85°C |
| APM32F030K8T6   | 64        | 8        | LQFP32  | 2500  | Industrial grade -40°C~85°C |
| APM32F030C6T6-R | 32        | 4        | LQFP48  | 2000  | Industrial grade -40°C~85°C |
| APM32F030C6T6   | 32        | 4        | LQFP48  | 2500  | Industrial grade -40°C~85°C |
| APM32F030C8T6-R | 64        | 8        | LQFP48  | 2000  | Industrial grade -40°C~85°C |
| APM32F030C8T6   | 64        | 8        | LQFP48  | 2500  | Industrial grade -40°C~85°C |
| APM32F030R8T6-R | 64        | 8        | LQFP64  | 1000  | Industrial grade -40°C~85°C |
| APM32F030R8T6   | 64        | 8        | LQFP64  | 1600  | Industrial grade -40°C~85°C |

Note :SPQ= Minimum number of packages

## 8. Packaging information

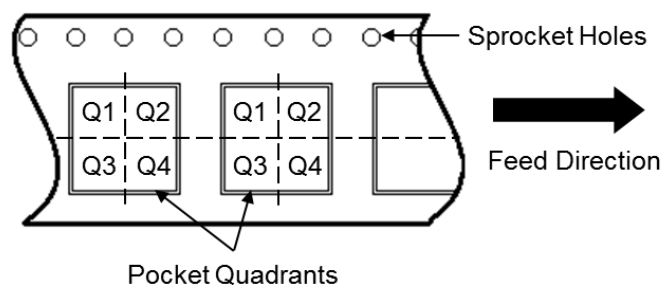
### 8.1. Reel packaging

Figure 39 Reel dimensions

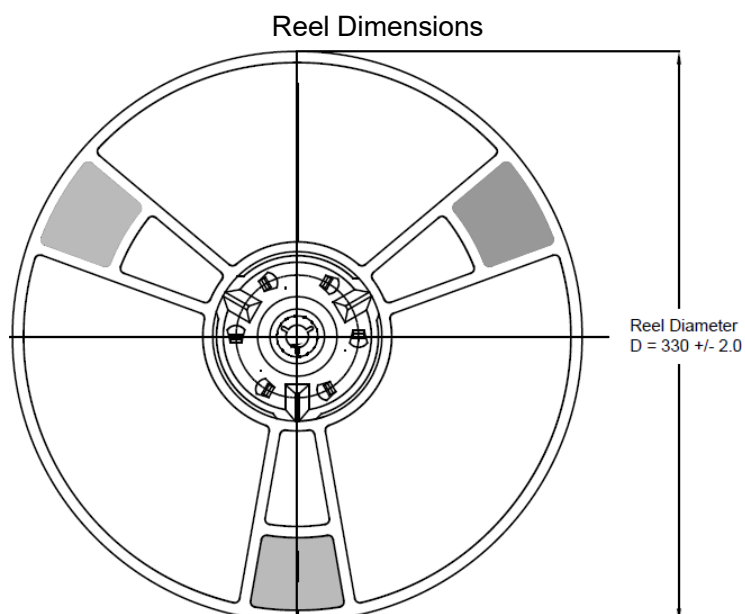


|    |                                                           |
|----|-----------------------------------------------------------|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |

Quadrant Assignments for PIN1 Orientation in Tape







**Table 57 Reel packaging parameter specification table**

| Device        | Package Type | Pins | SPQ  | Reel Diameter (mm) | A0 (mm) | B0 (mm) | K0 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|------|------|--------------------|---------|---------|---------|--------|---------------|
| APM32F030R8T6 | LQFP         | 64   | 1000 | 330                | 12.35   | 12.35   | 2.2     | 24     | Q1            |
| APM32F030C6T6 | LQFP         | 48   | 2000 | 330                | 9.3     | 9.3     | 2.2     | 16     | Q1            |
| APM32F030C8T6 | LQFP         | 48   | 2000 | 330                | 9.3     | 9.3     | 2.2     | 16     | Q1            |
| APM32F030K6T6 | LQFP         | 32   | 2000 | 330                | 9.3     | 9.3     | 2.2     | 16     | Q1            |
| APM32F030K8T6 | LQFP         | 32   | 2000 | 330                | 9.3     | 9.3     | 2.2     | 16     | Q1            |
| APM32F030K6U6 | QFN          | 32   | 5000 | 330                | 5.3     | 5.3     | 0.8     | 12     | Q1            |
| APM32F030F4P6 | TSSOP        | 20   | 4000 | 330                | 6.7     | 6.9     | 1.3     | 16     | Q1            |
| APM32F030F6P6 | TSSOP        | 20   | 4000 | 330                | 6.7     | 6.9     | 1.3     | 16     | Q1            |
| APM32F030F8P6 | TSSOP        | 20   | 4000 | 330                | 6.7     | 6.9     | 1.3     | 16     | Q1            |

## 8.2. Tray packaging

Figure 40 Tray packaging diagram

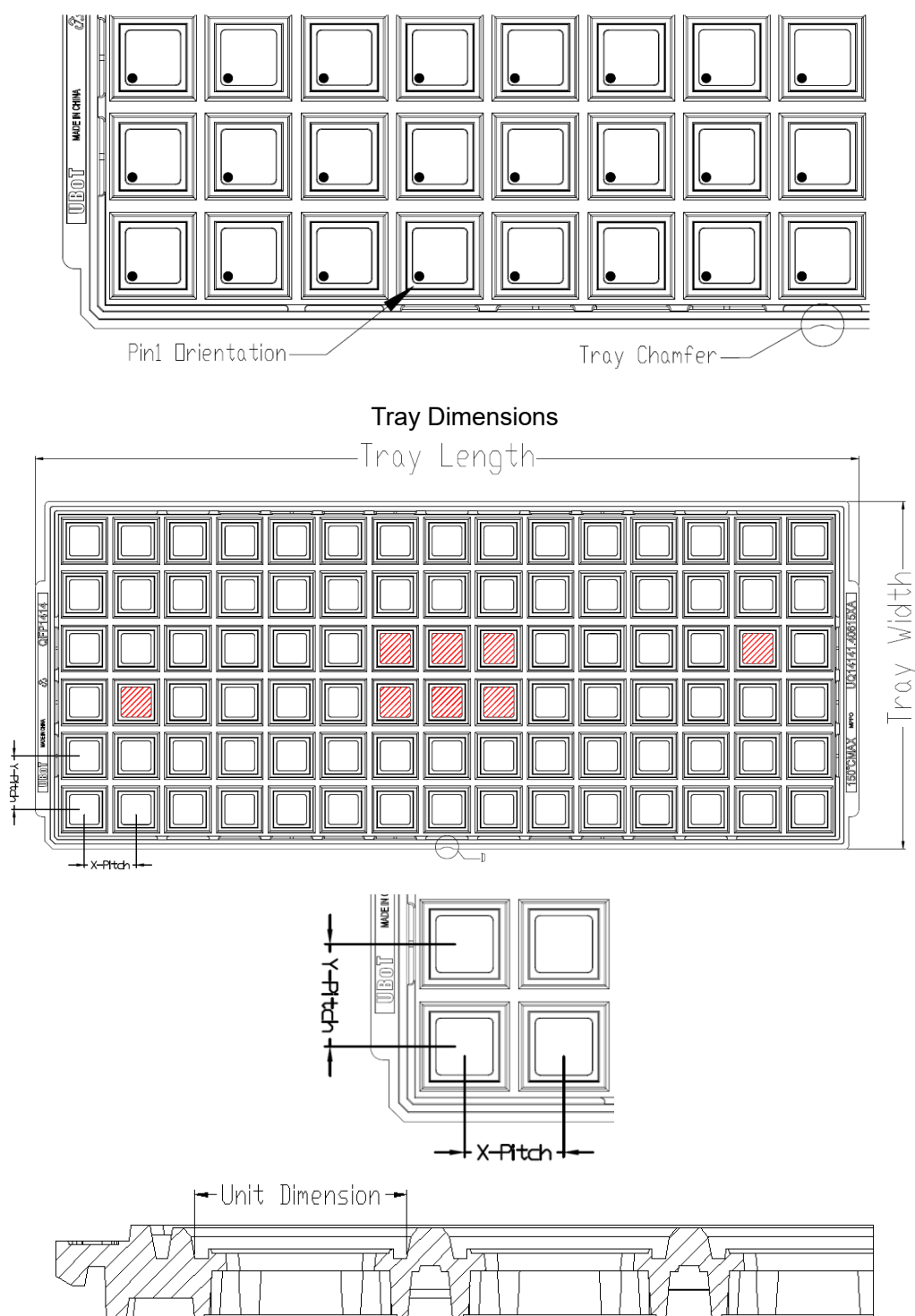


Table 58 Tray packaging parameter specification table

| Device | Package Type | Pins | SPQ | X-Dimension (mm) | Y-Dimension (mm) | X-Pitch (mm) | Y-Pitch (mm) | Tray Length (mm) | Tray Width (mm) |
|--------|--------------|------|-----|------------------|------------------|--------------|--------------|------------------|-----------------|
|--------|--------------|------|-----|------------------|------------------|--------------|--------------|------------------|-----------------|

|               |      |    |      |      |      |      |      |       |       |
|---------------|------|----|------|------|------|------|------|-------|-------|
| APM32F030R8T6 | LQFP | 64 | 1600 | 12.3 | 12.3 | 15.2 | 15.7 | 322.6 | 135.9 |
| APM32F030C6T6 | LQFP | 48 | 2500 | 9.7  | 9.7  | 12.2 | 12.6 | 322.6 | 135.9 |
| APM32F030C8T6 | LQFP | 48 | 2500 | 9.7  | 9.7  | 12.2 | 12.6 | 322.6 | 135.9 |
| APM32F030K6T6 | LQFP | 32 | 2500 | 9.7  | 9.7  | 12.2 | 12.6 | 322.6 | 135.9 |
| APM32F030K8T6 | LQFP | 32 | 2500 | 9.7  | 9.7  | 12.2 | 12.6 | 322.6 | 135.9 |
| APM32F030C6U6 | QFN  | 48 | 2600 | 7.25 | 7.25 | 11.8 | 12.8 | 322.6 | 135.9 |
| APM32F030C8U6 | QFN  | 48 | 2600 | 7.25 | 7.25 | 11.8 | 12.8 | 322.6 | 135.9 |
| APM32F030K6U6 | QFN  | 32 | 4900 | 5.2  | 5.2  | 8.7  | 9.0  | 322.6 | 135.9 |
| APM32F030G4U6 | QFN  | 28 | 4900 | 4.2  | 4.2  | 8.8  | 9.2  | 322.6 | 135.9 |
| APM32F030G6U6 | QFN  | 28 | 4900 | 4.2  | 4.2  | 8.8  | 9.2  | 322.6 | 135.9 |
| APM32F030G8U6 | QFN  | 28 | 4900 | 4.2  | 4.2  | 8.8  | 9.2  | 322.6 | 135.9 |

### 8.3. Material tube

Figure 41 Package drawing of material tube

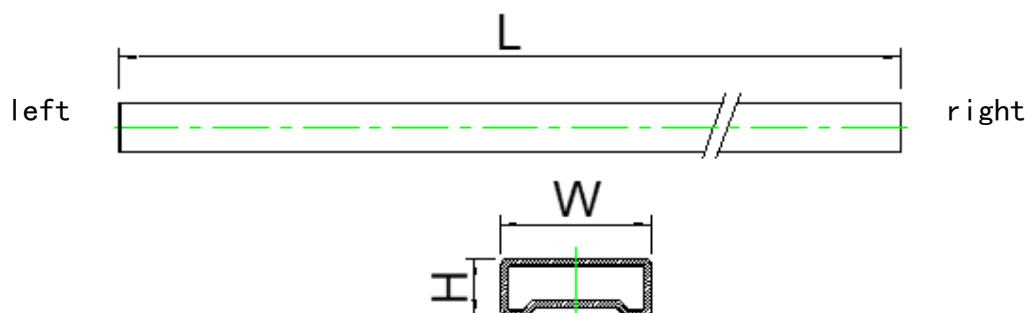


Table 59 Specification table of material tube packaging parameters

| Device        | Package Type | Pins | Qty Per Tube | SPQ   | L (mm) | W (mm) | H (mm) |
|---------------|--------------|------|--------------|-------|--------|--------|--------|
| APM32F030F8P6 | TSSOP        | 20   | 46           | 14720 | 327    | 8.5    | 3.2    |
| APM32F030F6P6 | TSSOP        | 20   | 46           | 14720 | 327    | 8.5    | 3.2    |
| APM32F030F4P6 | TSSOP        | 20   | 46           | 14720 | 327    | 8.5    | 3.2    |

## 9. Naming of common functional modules

Table 60 Naming of common functional modules

| Naming of common functional modules            |               |
|------------------------------------------------|---------------|
| Description in Chinese                         | Abbreviations |
| Reset management unit                          | RMU           |
| Clock management unit                          | CMU           |
| Reset and clock management unit                | RCM           |
| External interrupt                             | EINT          |
| Universal IO                                   | GPIO          |
| Multiplex IO                                   | AFIO          |
| Wake up controller                             | WUPT          |
| Buzzer                                         | BUZZER        |
| Independent watchdog timer                     | IWDT          |
| Window watchdog timer                          | WWDT          |
| Timer                                          | TMR           |
| CRC controller                                 | CRC           |
| Power management unit                          | PMU           |
| DMA controller                                 | DMA           |
| Digital analogue converter                     | ADC           |
| Real-time clock                                | RTC           |
| External memory controller                     | EMMC          |
| Controller area network                        | CAN           |
| I2C interface                                  | I2C           |
| serial peripheral interface                    | SPI           |
| Universal asynchronous transceiver             | UART          |
| Universal asynchronous synchronous transceiver | USART         |
| Flash interface control unit                   | FMC           |

## 10. Revision history

Table 62 Document revision history

| Date       | Revision | Change                                                                                                                                                                                                                                                                                                                                                                      |
|------------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2020.07.1  | V1.0.0   | New folder                                                                                                                                                                                                                                                                                                                                                                  |
| 2020.07.06 | V1.0.1   | Modify the cover page and directory format                                                                                                                                                                                                                                                                                                                                  |
| 2020.9.9   | V1.1     | (1) Modify the font<br>(2) Modify the naming rules of Order Information *(Chapter 7), modify the order code in the order Information list table and add a column of the minimum number of packages<br>(3) Modify the error in the Functional Description of APM32F030x4x6x8 Pin table<br>(4) Modify the Figure 27 Code Specification in the package information (Chapter 6) |
| 2021.6.4   | V1.2     | (1) Modify HXT-HSECLK<br>LXT-LSECLK<br>HIRC-HSICKL<br>LIRC-LSICKL<br>(2) modified LSECLK osc for crystal resonator to produce low speed.<br>(3) Modify the title of the recommended Layout diagram corresponding to QFN32.<br>(4) Delete the temperature sensor module                                                                                                      |
| 2021.6.30  | V1.3     | Increase the maximum rated current characteristic                                                                                                                                                                                                                                                                                                                           |
| 2022.3.9   | V1.4     | (1) Modify the last number of model 6 to X<br>(2) Delete the description of I2S in the DMA module<br>(3) Added pin function description note 1                                                                                                                                                                                                                              |
| 2022.5.7   | V1.5     | Modify some parameters                                                                                                                                                                                                                                                                                                                                                      |